26V, 4-Channel Voltage Bus and 4-Channel High-Side Current Shunt Monitor

NCP45495

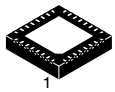
The NCP45495 is a high−performance monolithic IC which can be used to monitor bus voltage and current on four high−voltage power supplies simultaneously. The HV bus voltages and currents are translated to a low−voltage power domain and multiplexed onto a single differential output for measurement externally by common ADCs. The NCP45495 offers programmable voltage and current gain settings and requires a minimal amount of external passives for a small cost saving solution. The device is also configurable to operate either standalone or as a pair, permitting up to eight separate HV power supplies to be monitored and measured.

Features

- Translates and Scales Shunt and Bus Voltages up to 26 V
- Single Device Monitors Four Supplies
- May Be Paired for Monitoring Up To Eight Supplies
- Very Low Powerdown Current
- All Channels Individually Gain Programmable via I^2C Interface
- Fast Settling Time
- Real−Time Bus Voltages Valid Signal
- Adjustable Output Common−Mode Voltage
- RoHS/REACH Compliant Device

Applications

- Computers / Notebooks / Graphics Cards
- Power Management / Power Control Loops
- Battery Chargers

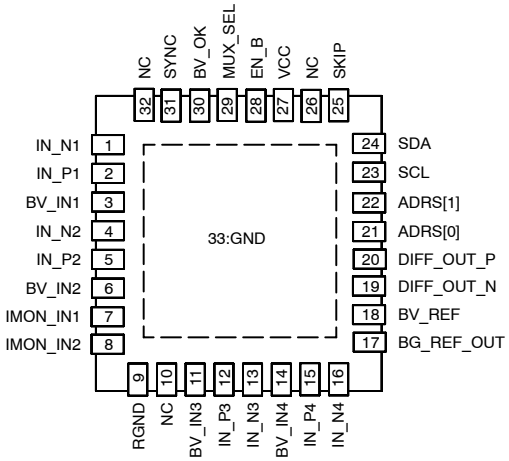


QFN32 4x4
CASE 485CD

MARKING DIAGRAM

45495	= Specific Device Code
A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
▪	= Pb−Free Package

PIN CONFIGURATION



(Top View)

ORDERING INFORMATION

Device	Package	Shipping†
NCP45495XMNTWG	QFN32 (Green)	4000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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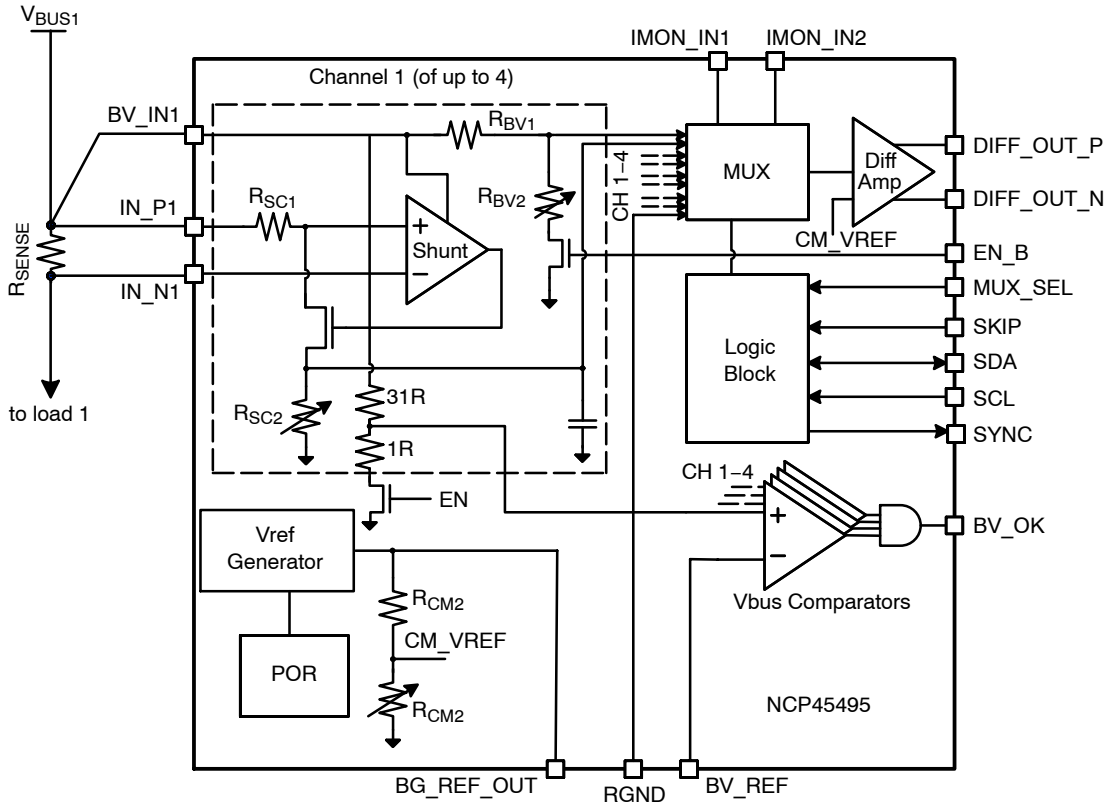


Figure 1. Block Diagram

Table 1. PIN DESCRIPTION

Pin	Name	I/O	Function
1,4,13,16	IN_Nx	AI	Sense Resistor Sense −, High Voltage
2,5,12,15	IN_Px	AI	Sense Resistor Sense +, High Voltage
3,6,11,14	BV_INx	AI	Bus Voltage Input for Voltage monitoring
7,8	IMON_INx	AI	Current Monitor Channels (High impedance input)
9	RGND	GND	Reference Ground for multiplexer and differential amplifier
17	BG_REF_OUT	AO	Buffered Bandgap Voltage Output
18	BV_REF	AI	BV_OK comparator threshold reference
19	DIFF_OUT_N	AO	Differential Output, Negative
20	DIFF_OUT_P	AO	Differential Output, Positive
21,22	ADRS[1:0]	DI	I^2C Address set bits
23	SCL	DI	I^2C Clock
24	SDA	DI/DO	I^2C Data Signal
25	SKIP	DI	Skip Function control (see description) Mask for BV_OK. High level is V_{CC} and low level is GND
27	VCC	PWR	Device Power
28	EN_B	DI	Device Enable. When high, places device in low−power state.
29	MUX_SEL	DI	Multiplexer Select Input
30	BV_OK	DO	Bus OK output (open−drain; high impedance = BUS OK)
31	SYNC	DO	Sync pin outputs a pulse at the beginning of every MUX_SEL sequence
33	GND	GND	Device Ground

Table 2. MAXIMUM RATINGS

Rating	Pins	Condition	Symbol	Value	Unit
Supply Voltage Range	VCC	GND = 0 V	V_{CC}	−0.3 to 5.5	V
Bus Input Voltage Range	BV_INx, IN_Px, IN_Nx	GND = 0 V	V_{BV_IN}	−0.3 to 30	V
Digital Input Voltage Range	MUX_SEL, EN_B, SKIP, SCL, SDA, ADRS[x]	GND = 0 V	V_{LV}	−0.3 to 5.5	V
Low Voltage I/O Range	DIFF_OUT_P, DIFF_OUT_N, BV_OK, BG_REF_OUT	GND = 0 V	V_{LV}	−0.3 to 5.5	V
Thermal Resistance, Junction−to−Air			$R_{\theta JA}$	40	°C/W
Thermal Resistance, Junction−to−Case (V_{IN} Paddle)			$R_{\theta JC}$	5	°C/W
Operating Temperature Range			T_{A1}	−40 to 105	°C
Functional Temperature Range			T_{A2}	−40 to 125	°C
Maximum Junction Temperature			T_J	125	°C
Storage Temperature Range			T_{STG}	−40 to 150	°C
Lead Temperature, Soldering (10 sec.)			T_{SLD}	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Table 3. ESD RATINGS

Rating	Symbol	Value	Unit
ESD Capability, Human Body Model (Note 1)	ESD_{HBM}	>2.0	kV
ESD Capability, Charged Device Model (Note 1)	ESD_{CDM}	>0.5	kV

1. Tested by the following methods @ T_A = 25°C
   ESD Human Body Model tested per AEC−Q100−002 (EIA/JESD22−A114)
   ESD Charged Device Model per JESD22−C101

Table 4. RECOMMENDED OPERATING RANGES

Rating	Symbol	Min	Max	Unit
Supply Voltage Range	V_{CC}	2.8	3.8	V
Bus Input Pin Voltage Range	V_{IN_PX}, V_{IN_Nx}	5	26	V
Digital Input High Voltage Range (Note 2)	V_{IH}	0.945		V
Digital Input Low Voltage Range (Note 2)	V_{IL}		0.405	V
SKIP Input High Voltage Range	$SKIP_{VIH}$	2.8	3.8	V
SKIP Input Low Voltage Range	$SKIP_{VIL}$		0.405	V
Ambient Temperature	T_A	−40	85	°C
Junction Temperature	T_J	−40	125	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

2. V_{IL} and V_{IH} ranges apply to the EN_B, SCLK, SDA, ADRS[x], and MUX_SEL pins

Table 5. ELECTRICAL CHARACTERISTICS V_{IN_PX} = 15 V, V_{EN_B} = 0 V, Vcc = 3.3 V, unless indicated otherwise. Min and Max values are valid for temperature range −40°C < T_J < +105°C unless noted otherwise and are guaranteed by test, design, characterization, or statistical correlation. Typical values are referenced to T_J = 25°C

Parameter	Symbol	Min	Typ	Max	Unit
AC CHARACTERISTICS (T_J = 25°C unless otherwise specified)					
Multiplexer Settling Time (to 9.375 mV)	T_{STAB1}			100	ns
Multiplexer Settling Time (to 3 mV)	T_{STAB2}			300	ns
MUX_SEL Period (normal operation – assuming no timeout set)	T_{MSP}	0.185			μs
MUX_SEL Timeout (from falling edge of MUX_SEL)		35	39	43	μs
Power−up Time (STANDBY or Limited Function to Full Function) (Note 3)	T_{PWR_UP}			40	μs
Differential Amplifier Capacitive Load Capability (Note 4)	C_{DIFF}			82	pF
DC CHARACTERISTICS					
Input Impedance (EN_B pin tri−stated)	R_{FLOAT}	100k			Ω
IMONx Channel Input Leakage Current				100	nA
BG_REF_OUT Voltage	V_{BG}	1.274	1.3	1.326	V
BG_REF_OUT maximum loading	I_{BG}			100	μA
BV_OK Logic Low Impedance (Note 5)	R_{BV_OK}			300	Ω
BV_REF Voltage Range	BV_REF	100		800	mV
BV_OK Comparator Hysteresis		7.5	10	12.5	%
BV_OK Comparator VBUS divide ratio			1/32		V/V
VCC range for BV_OK low impedance	V_{LI}	1		3.8	V
VCC Threshold Reference for BV_OK Input (POR) (Note 6)	V_{BV_TH}	2.6		2.8	V
POR Hysteresis			150		mV
Shunt Monitor Offset Voltage, room temp (Note 7)	V_{SM_OV}	−150		150	μV
Shunt Monitor Offset Voltage Drift (Note 7)	SM_VD			2	μV/°C
Shunt Monitor CMRR (V_{IN_Px} in valid range, see above)	SM_CMRR	80			dB
Shunt Current Gain Range (See Table 6)		2		24	V/V
Shunt Current Gain Tolerance (Note 11)				0.6	%
Differential Amp Input Offset Voltage, 25°C (Note 8)	V_{D_OVRT}	−2		2	mV
Differential Amp Input Offset Voltage, −40°C to 105°C (Note 8)	V_{D_OVT}	−6		6	mV
Differential Amp PSRR (V_{CC} = 2.8 V to 3.8 V)	DA_PSRR	54			dB
Differential Amp Common−Mode Voltage	V_{CMR}	575		875	mV
Differential Amp Closed Loop Gain (Note 11)	G_{DA}	0.994	1	1.006	V/V
Differential Full Scale Output	V_{FSO}			800	mV_{pp}
I_VCC (Fully Functional, EN_B = 0, MUX_SEL clocked at 2 MHz, VCC must be 2.8 V – 3.8 V)	I_{VCC_F}			2.0	mA
I_VCC (Limited Function, EN_B=Tristate, VCC must be 2.8 V = 3.8 V)	I_{VCC_L}			400	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. T_{PWR_UP} begins when EN_B goes low. After the power up time, MUX_SEL may begin clocking out data. This time also applies following any register programming.
4. Differential Output C_{LOAD} (i.e.: DIFF_OUT_x to GND) appears as a series RC with lumped equivalent R (0.86−8.6 Ω)
5. BV_OK should be connected to a pull up resistor of value 10 KΩ or greater.
6. Vcc detection for BV_OK must trip in this range. Device can be either Full Function or Limited Function mode in this range
7. Shunt Monitor Offset Voltage and Offset Voltage Drift are referred to the IN_Px and IN_Nx pins.
8. Differential Amplifier Input Offset Voltage is referred to the multiplexer input pins
9. V_{EN} = V_{CC}; Total V_{CC} standby current is I_{VCC_S} for every IN_Px channel that is not floating
10. Specifications for V_{BUS} current draw are only applicable when V_{CC} = 2.8 V to 3.8 V.
11. 3−sigma variation specification

Table 5. ELECTRICAL CHARACTERISTICS V_{IN_PX} = 15 V, V_{EN_B} = 0 V, Vcc = 3.3 V, unless indicated otherwise. Min and Max values are valid for temperature range −40°C < T_J < +105°C unless noted otherwise and are guaranteed by test, design, characterization, or statistical correlation. Typical values are referenced to T_J = 25°C

Parameter	Symbol	Min	Typ	Max	Unit
DC CHARACTERISTICS					
I_VCC (STANDBY) (Note 9)	I_{VCC_S}			200	μA
I_BV_IN (BV_IN current in STANDBY mode)	$I_{BV_IN_S}$			2	μA
I_BV_IN (BV_IN current in LIMITED mode)	$I_{BV_IN_L}$			120	μA
I_BV_IN (BV_IN current in Full Function)	$I_{BV_IN_F}$			600	μA
I_BV_IN (BV_IN current when VCC = FLOATING)	I_{BV_IN}			2	μA
I_IN_N (IN_N current in STANDBY/LIMITED mode) (Note 10)	I_{IN_N}			1	μA
I_IN_P (IN_P current in STANDBY/LIMITED mode) (Note 10)	I_{IN_P}			1	μA
I_IN_N (IN_N current in Full Function mode) (Note 10)				60	μA
I_IN_P (IN_P current in Full Function mode mode) (Note 10)				60	μA
V_{BUS} Gain Range		1/64		1/4	V/V
V_{BUS} Gain Tolerance				0.6	%

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. T_{PWR_UP} begins when EN_B goes low. After the power up time, MUX_SEL may begin clocking out data. This time also applies following any register programming.
4. Differential Output C_{LOAD} (i.e.: DIFF_OUT_x to GND) appears as a series RC with lumped equivalent R (0.86−8.6 Ω)
5. BV_OK should be connected to a pull up resistor of value 10 KΩ or greater.
6. Vcc detection for BV_OK must trip in this range. Device can be either Full Function or Limited Function mode in this range
7. Shunt Monitor Offset Voltage and Offset Voltage Drift are referred to the IN_Px and IN_Nx pins.
8. Differential Amplifier Input Offset Voltage is referred to the multiplexer input pins
9. $V_{EN} = V_{CC}$; Total V_{CC} standby current is I_{VCC_S} for every IN_Px channel that is not floating
10. Specifications for V_{BUS} current draw are only applicable when V_{CC} = 2.8 V to 3.8 V.
11. 3−sigma variation specification

DETAILED DESCRIPTION

Differential Output Amplifier: An integrated differential output amplifier provides a scaled representation of multiple bus voltages and currents to an external ADC on the DIFF_OUT_P and DIFF_OUT_N pins. These voltages and currents are presented *sequentially* (under control of the Sequence Logic block) via the Multiplexer. The gain of the differential amplifier is 1 V/V. The common−mode voltage of the differential output amplifier is established by an internal reference divider. The common mode voltage is programmable from 575 mV to 875 mV in 25 mV increments to offer flexibility for the ADC reading the differential outputs. The contents of the DIFF_AMP_CM register set the differential amplifier common mode voltage. The offset of the differential amplifier is also programmable by setting the DIFF_AMP_OFFSET register. The differential offset can be set to 0 mV or from −325 to −375 mV in 25 mV increments. See the DIFF_AMP register description in the I^2C interface definition section for more details.

Shunt Current Monitor (one of four identical instances): The differential voltage across an external sense resistor (R_{SENSE}) is converted to a current by a transconductor stage implemented by an op−amp and an internal shunt resistor R_{SC1}. The current is forced through a programmable internal resistor R_{SC2} to create the internal shunt voltage. The resulting voltage is fed into the multiplexer for readout. The conversion gain can be programmed to gains from 2x to 24x. The SHUNT_GAINx registers are used to set the shunt current gains for each channel. The voltage represented on the differential output for the shunt current is the voltage drop across the external sense resistor multiplied by the shunt gain.

*Diff Output = Iload * Rsense * shunt gain*

The table below shows the available shunt gain settings.

Table 6. SHUNT CURRENT PROGRAMMABLE GAIN SETTINGS

SHUNT_GAIN (Bits 5−1)	Register Contents (includes bit 0)	Shunt Current Channel Gains
0b'11111	0x3E	24.000
0b'11110	0x3C	22.151
0b'11101	0x3A	20.445
0b'11100	0x38	18.870
0b'11011	0x36	17.417
0b'11010	0x34	16.075
0b'11001	0x32	14.837
0b'11000	0x30	13.694
0b'10111	0x2E	12.639
0b'10110	0x2C	11.665
0b'10101	0x2A	10.767
0b'10100	0x28	9.937
0b'10011	0x26	9.172
0b'10010	0x24	8.465
0b'10001	0x22	7.813
0b'10000	0x20	7.212
0b'01111	0x1E	6.656
0b'01110	0x1C	6.143
0b'01101	0x1A	5.670
0b'01100	0x18	5.233
0b'01011	0x16	4.830
0b'01010	0x14	4.458
0b'01001	0x12	4.115
0b'01000	0x10	3.798
0b'00111	0x0E	3.505
0b'00110	0x0C	3.235
0b'00101	0x0A	2.986
0b'00100	0x08	2.756
0b'00011	0x06	2.544
0b'00010	0x04	2.348
0b'00001	0x02	2.167
0b'00000	0x00	2.000

Bus Voltage Monitor (one of four identical instances): An internal voltage divider (R_{BV1} and R_{BV2}) is used to scale the voltage on the BV_INx pin to an appropriate full−scale range for the differential output amplifier. The voltage divider is programmable from 1/4(V/V) to 1/64(V/V) as shown in the table below. BUS_GAINx registers are used to set the voltage gains for each channel. The differential output voltage representing the bus voltage is the bus voltage divided by the VBUS attenuation.

$$\text{Diff Output} = \frac{V_{BUS}}{A_V}$$

Table 7. VBUS PROGRAMMABLE ATTENUATION SETTINGS

BUS_GAIN (Bits 5−1)	Register Contents (includes bit 0)	VBUS Attenuation Setting (A_V)
0b'00000	0x00	64.00
0b'00001	0x02	58.524
0b'00010	0x04	53.517
0b'00011	0x06	48.939
0b'00100	0x08	44.752
0b'00101	0x0A	40.923
0b'00110	0x0C	37.422
0b'00111	0x0E	34.220
0b'01000	0x10	31.292
0b'01001	0x12	28.615
0b'01010	0x14	26.167
0b'01011	0x16	23.928
0b'01100	0x18	21.881
0b'01101	0x1A	20.009
0b'01110	0x1C	18.297
0b'01111	0x1E	16.732
0b'10000	0x20	15.300
0b'10001	0x22	13.991
0b'10010	0x24	12.794
0b'10011	0x26	11.700
0b'10100	0x28	10.699
0b'10101	0x2A	9.783
0b'10110	0x2C	8.946
0b'10111	0x2E	8.181
0b'11000	0x30	7.481
0b'11001	0x32	6.841
0b'11010	0x34	6.256
0b'11011	0x36	5.720
0b'11100	0x38	5.231
0b'11101	0x3A	4.783
0b'11110	0x3C	4.374
0b'11111	0x3E	4.000

High Impedance Voltage Monitor (one of two identical instances):

The voltage on the IMON_INx pin is fed directly to the multiplexer for readout. The differential output voltage represents the voltage on the IMON_INx pin.

Multiplexer Select: The multiplexer selection is controlled by a single digital input (MUX_SEL pin). The device will monitor this pin and cycle through the different measured parameters in a fixed sequence. The sequence will repeat the cycle until either a timeout condition is detected or the device is disabled. If the timeout is disabled, then MUX_SEL must be clocked through the whole sequence before the cycle will repeat.

MUX_SEL Timeout

The MUX_SEL timeout can be enabled or disabled over the I^2C interface. If enabled, after 45 μs of idle time on the MUX_SEL pin the MUX_SEL sequence is reset back to the beginning. All new register settings will become effective at the timeout. Writing 0b1 to the TIMEOUT register will disable the timeout. If the timeout is disabled, MUX_SEL must be clocked to complete the full sequence before the cycle will repeat.

Paired Devices: In paired operation, programmed bits in the MUX_SEL_SKIP register designate which device is "Device A" and "Device B" of a pair. Device A always goes first in the sequence. When paired, the differential output amplifiers of the two devices are expected to be "wire−or'ed" together, and the table logic insures that only one device will actively drive the output pins DIFF_OUT_P and DIFF_OUT_N at any given time. See description in the Auxiliary Functions section for details. When in paired mode, the configuration register settings for registers TIMEOUT, DIFF_AMP_OFFSET and DIFF_AMP_CM must match between the 2 devices.

Power−up Sequence

Correct functionality of the power monitor is not dependent on a specific power up sequence. All used bus voltages and VCC must be powered before the output will be correct. The ACTIVE_CHAN register must be set over the I^2C interface after VCC is up to set the active channel count. MUX_SEL may begin clocking out data 40us after EN_B goes low. Before the part is configured, BV_OK will function with all VBUS channels considered active. Because all VBUS channels are active by default until otherwise configured, if BV_OK functionality is used before the part is configured, un−used VBUS inputs should be tied to used VBUS inputs.

Calibration Cycle

Setting bit 7 in the ACTIVE_CHAN register adds an additional cycle at the end of the standard MUX_SEL cycles. During this cycle, the device ground (connected to the RGND pin) is muxed through the signal chain. The

resulting differential output represents the differential amplifier offset error. The RGND pin should be treated as a reference ground. The controller can use the RGND readout to cancel out remaining offset error if desired. The calibration cycle is disabled by default. If in paired mode with 2 devices, then a calibration cycle will be added to the end of the sequence from each individual contributing device respectively. See Figure 2 and Figure 10 for CAL cycle example.

Polarity Mode

Setting bit 7 in the ALTERNATING_MODE register puts the differential output in alternating polarity mode. In alternating polarity mode, the voltage and current readouts will be repeated with alternating differential amplifier input polarity. This allows the user to compute and cancel out any differential amplifier offset. An example of an output using polarity mode is shown in the application section. Polarity mode is disabled by default. If in paired mode, the alternating polarity cycles will be added for each individual device output.

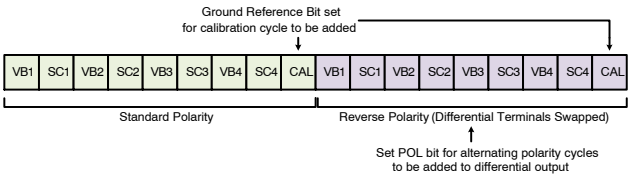


Figure 2. Sequence Showing Differential Output Format Options

SYNC Signal

The SYNC output pin pulses high for the first MUX_SEL period in a MUX_SEL sequence beginning with the second MUX_SEL sequence and continuing for all subsequent cycles. This is useful for the user to ensure synchronization, to guarantee the right channels are sampled at the right time. The SYNC pin is particularly useful for applications where MUX_SEL is clocked continuously. When devices are used in paired mode, the SYNC signal for each device will be relative to its own position in the sequence.

I²C INTERFACE DETAILS

The NCP45495 uses a 400 kHz, slave mode FM I²C interface for communication with an I²C master. The purpose of the I²C interface is to provide access to configuration settings. Data packets for the power monitor I²C interface are sent with a 7 bit slave address, an 8 bit register address, a read / write bit, and 8 bits of data. Acknowledge bits are used after the addresses and data as a handshake verification. The address for the device can be set to one of 4 available addresses using the ADRS[1:0] pins. If in paired mode, Device A's address must be different than Device B's address. Continuous read and continuous write I²C modes, or combined formats are not supported by the NCP45495. Bits are always sent out MSB first.

The ADRS[1:0] address mapping is as follows:

ADRS[1]	ADRS[0]	Set Device Address
0	0	0x34
0	1	0x35
1	0	0x36
1	1	0x37

It is recommended that all necessary registers are programmed while EN_B is held high. On the falling edge of EN_B, the programmed registers will be committed. On the first rising edge of the first MUX_SEL, the register setting will be effective. If register settings are programmed after EN_B has been asserted low, then the new settings will be effective at the beginning of the next MUX_SEL cycle. If register settings are programed while MUX_SEL is running, then the new settings will be effective on the rising edge of the first MUX_SEL of the next cycle.

The I²C bus can also be locked by setting the appropriate bits in the LOCK register. Setting bit 1 will lock the I²C interface to any write commands. In this configuration, the device will respond to read commands, but not to write commands. Setting bit 0 will lock the I²C interface completely. In this configuration the device will not respond to any I²C activity. The device must be power cycled to get out of either of these locked states.

CONFIGURATION EXAMPLES

Figure 3 below shows an example of a register write. In this example, the address pins of the NCP45495 are tied low, selecting address 0x34 as the slave address. The ACITVE_CHAN register is written with 0x89, which will set channel 1 and channel 4 active, the ground reference is also enabled.

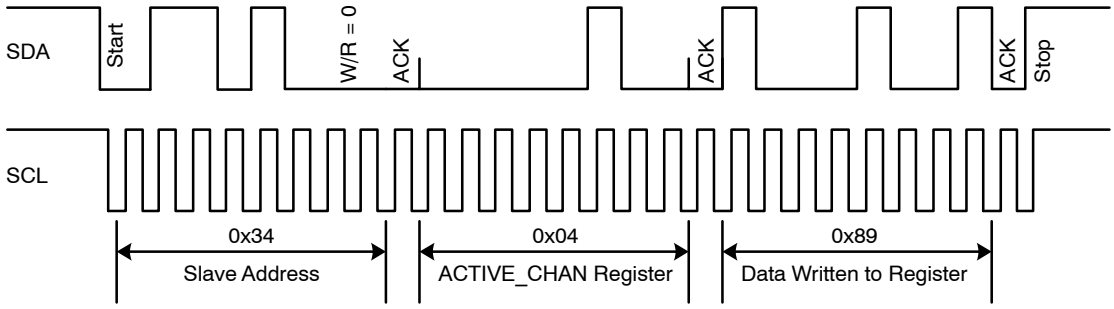


Figure 3. I²C Register Write Example

Figure 4 below shows an example of a register read. In this example, the master reads 0x89 from the ACTIVE_CHAN register.

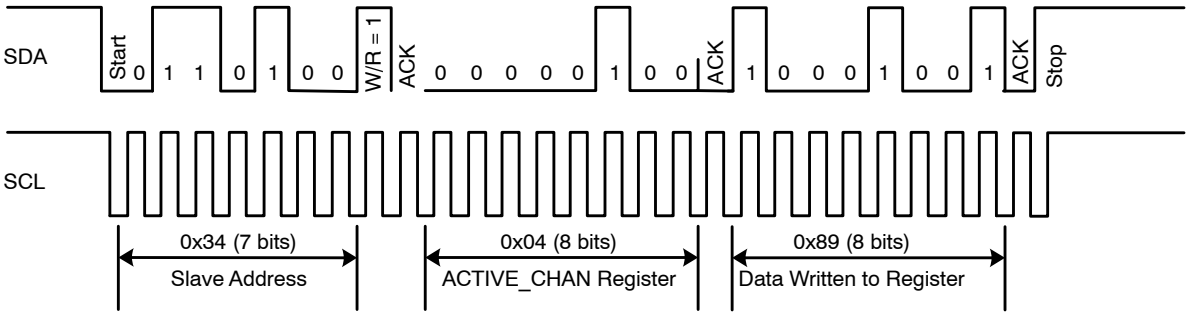


Figure 4. I²C Register Read Example

Table 8. TIMING REQURIEMENTS: I²C INTERFACE

Rating	Symbol	Min	Max	Unit
SCL Clock Frequency	F_{I2C}		0.4	MHz
Repeated hold time START condition (after this period, the first clock pulse is generated)	$t_{HD,STA}$	0.26	–	μs
Data hold time	$t_{HD,DAT}$	0	–	μs
LOW period of the SCL clock	t_{LOW}	0.5	–	μs
HIGH period of the SCL clock	t_{HIGH}	0.26	–	μs
Setup time for repeated start condition	$t_{SU,STA}$	0.26	–	μs
Data setup time	$t_{SU;DAT}$	50	–	ns
Rise time for both SDA and SCL signals	t_r	–	120	ns
Fall time of both SDA and SCL signals	t_f	18.1	120	ns
Setup time for STOP condition	$t_{SU,STO}$	0.26	–	μs
Bus free time between a STOP and START condition	t_{BUF}	0.5	–	μs
Capacitive load for each bus line	C_B	–	550	pF
Noise margin at the LOW level for each connected device	V_{nL}	$0.1*V_{CC}$	–	V
Noise margin at the HIGH level for each connected device	V_{nH}	$0.2*V_{CC}$	–	V
Max ACK delay	ACK_{MAX}		1	ms

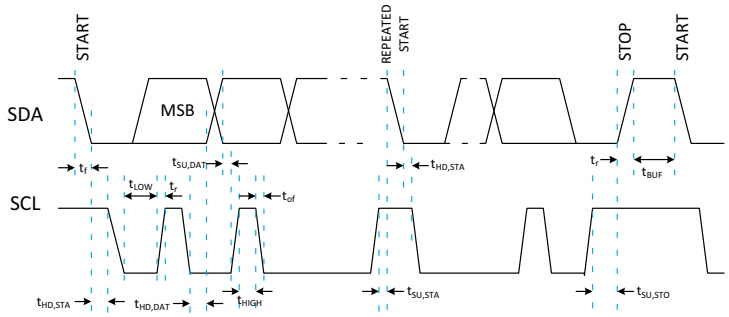


Figure 5. I²C Bus Timing

Write Data Example

1 bit	7 bits	1 bit	1 bit	8 bits	1 bit	8 bits	1 bit	1 bit
S	Slave Address	W=0	A	Register Address	A	DATA	A/$\overline{A}$	P

Read Data Example

1 bit	7 bits	1 bit	1 bit	8 bits	1 bit	8 bits	1 bit	1 bit
S	Slave Address	R=1	A	Register Address	A	DATA	A/$\overline{A}$	P

From master to slave

From slave to master

- A = acknowledge (SDA low)
- $\overline{A}$ = Not acknowledge (SDA high)
- S = START condition
- P = STOP condition

Figure 6. I²C Read / Write Protocol Format

Repeated Start format is also supported as shown below.

Read Data Example with Repeated Start

1 bit	7 bits	1 bit	1 bit	8 bits	1 bit	1 bit	7 bits	1 bit	1 bit	8 bits	1 bit	1 bit
S	Slave Address	R=0	A	Register Address	A	Sr	Slave Address	R=1	A	DATA	A/$\overline{A}$	P

Repeated Start

From master to slave

From slave to master

- A = acknowledge (SDA low)
- $\overline{A}$ = Not acknowledge (SDA high)
- S = START condition
- P = STOP condition

Figure 7. I²C Read with Repeated Start Format

The purposes and utilities of all accessible registers in the NCP45495 are detailed below. Addresses and bit assignments are explained.

Table 9. REGISTER MAP

Register Address	Register Name	Bits	R/W	Description	Default Setting	New Value Takes Effect
0x00	VendorID	7:0	R	**onsemi** Specific ID	0x4F	N/A
0x01	DeviceID	7:0	R	NCP45495 Specific Device ID	0x2D	N/A
0x04	ACTIVE_CHAN	7	R/W	Enable Ground Reference	0	At next MUX_SEL cycle
		5	R/W	Enable iMon Channel 2	0	At next MUX_SEL cycle
		4	R/W	Enable iMon Channel 1	0	At next MUX_SEL cycle
		3	R/W	Enable Channel 4	1	At next MUX_SEL cycle
		2	R/W	Enable Channel 3	1	At next MUX_SEL cycle
		1	R/W	Enable Channel 2	1	At next MUX_SEL cycle
		0	R/W	Enable Channel 1	1	At next MUX_SEL cycle
0x05	MUX_SEL_SKIP (set as 0x00 if operating in single device mode)	7:4	R/W	Pulses to skip at the start of the MUX_SEL cycle (skipping pulses at the beginning defines device as device B in paired mode)	0x0	At next MUX_SEL cycle
		3:0	R/W	Pulses to skip at the end of the MUX_SEL cycle (skipping pulses at the end defines device as device A in paired mode)	0x0	At next MUX_SEL cycle
0x06	ALTERNATING_MODE	7:7	R/W	0b1: Use Alternating Polarity Mode 0b0: Alternating Polarity Mode Disabled	0	At next MUX_SEL cycle
0x07	DIFF_AMP_OFFSET	1:0	R/W	0b11: −375 mV 0b10: −350 mV 0b01: −325 mV 0b00: 0 mV	0x0	Immediately
0x08	DIFF_AMP_CM Note: Differential output accuracy not guaranteed with V_{CMR} below 575 mV. (Codes 0x0, 0x1, 0x2)	3:0	R/W	0b1111: 875 mV 0b1110: 850 mV 0b0111: 675 mV 0b0100: 600 mV 0b0011: 575 mV	0x7 (675mV)	Immediately
0x0F	TIMEOUT	7:7	R/W	0b1: Disable Timeout 0b0: Timeout Active	0	Immediately
0x10	BUS_GAIN1	5:1	R/W	(Register contents: See Table 7) 0x3E: 1/4 0x00: 1/64	0x00 (1/64)	Immediately
0x11	BUS_GAIN2	5:1	R/W			
0x12	BUS_GAIN3	5:1	R/W			
0x13	BUS_GAIN4	5:1	R/W			
0x20	SHUNT_GAIN1	5:1	R/W	(Register contents: See Table 6) 0x3E: 24x 0x00: 2x	0x00 (2x)	Immediately
0x21	SHUNT_GAIN2	5:1	R/W			
0x22	SHUNT_GAIN3	5:1	R/W			
0x23	SHUNT_GAIN4	5:1	R/W			
0x24	LOCK	1	R/W	Lock I^2C interface writes	0	Immediately
		0	R/W	Lock I^2C interface reads / writes	0	Immediately

APPLICATIONS DIAGRAMS

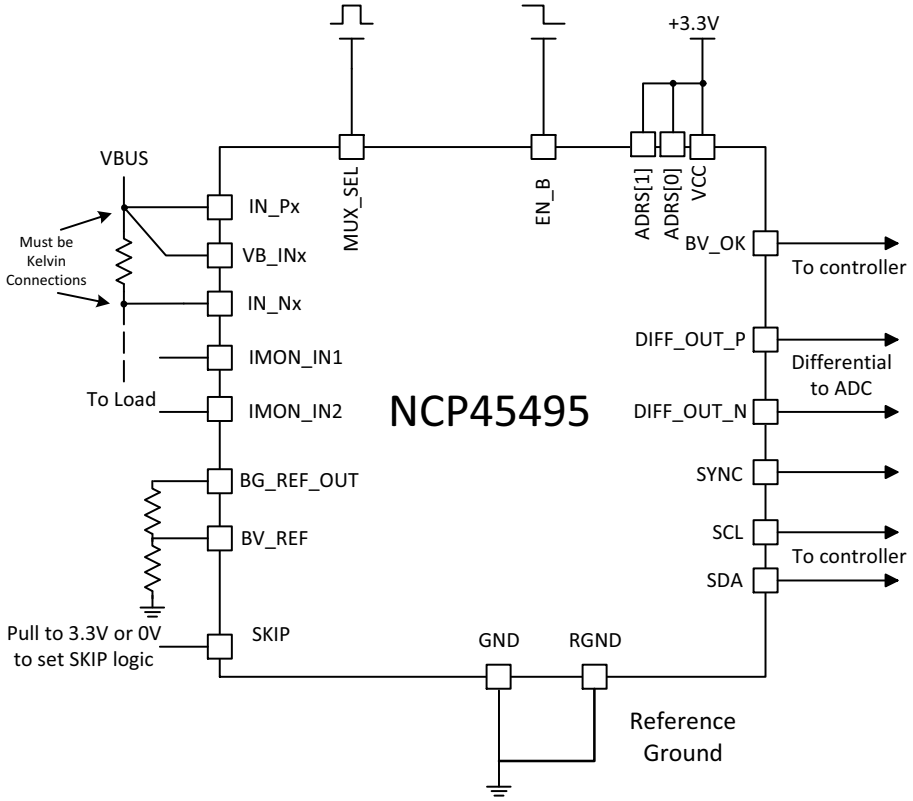


Figure 8. Stand Alone Device Typical Application Diagram

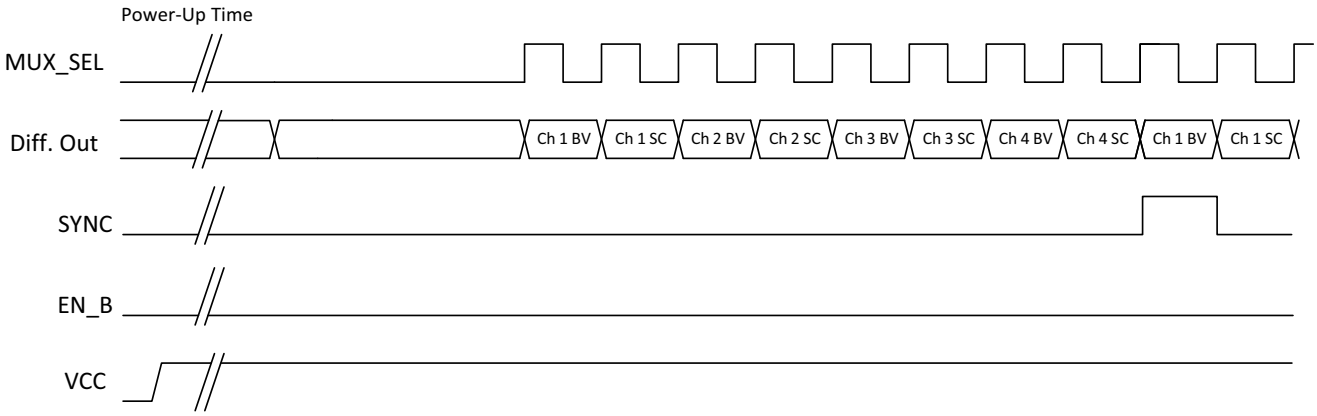


Figure 9. Stand Alone Signal Characteristics with all 4 Channels Activated

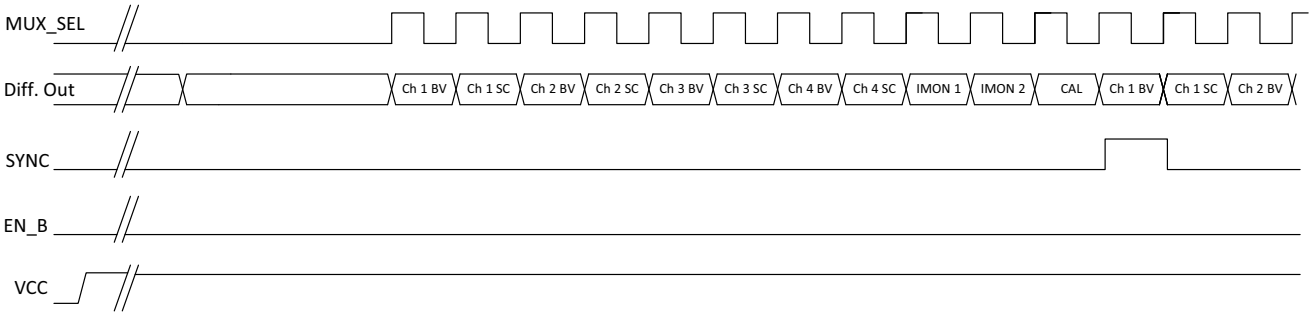


Figure 10. Stand Alone Signal Characteristics with IMON 1, IMON2, and Ground Reference Bits Set and all Channels Activated

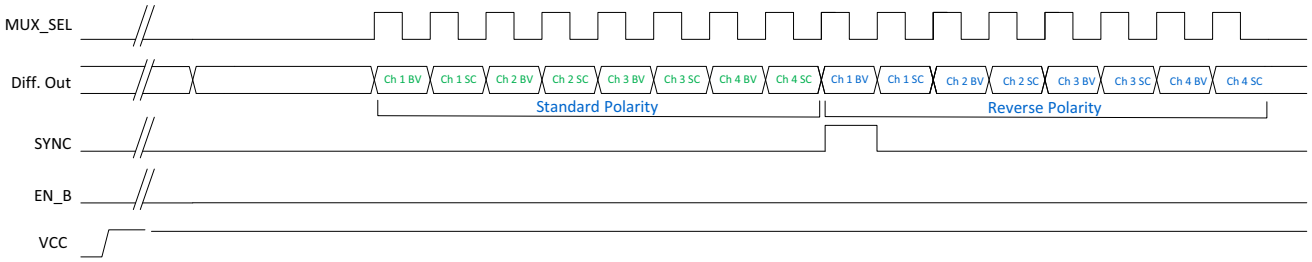


Figure 11. Stand Alone Signal Characteristics with ALTERNATING_MODE Bit Set and all Channels Activated

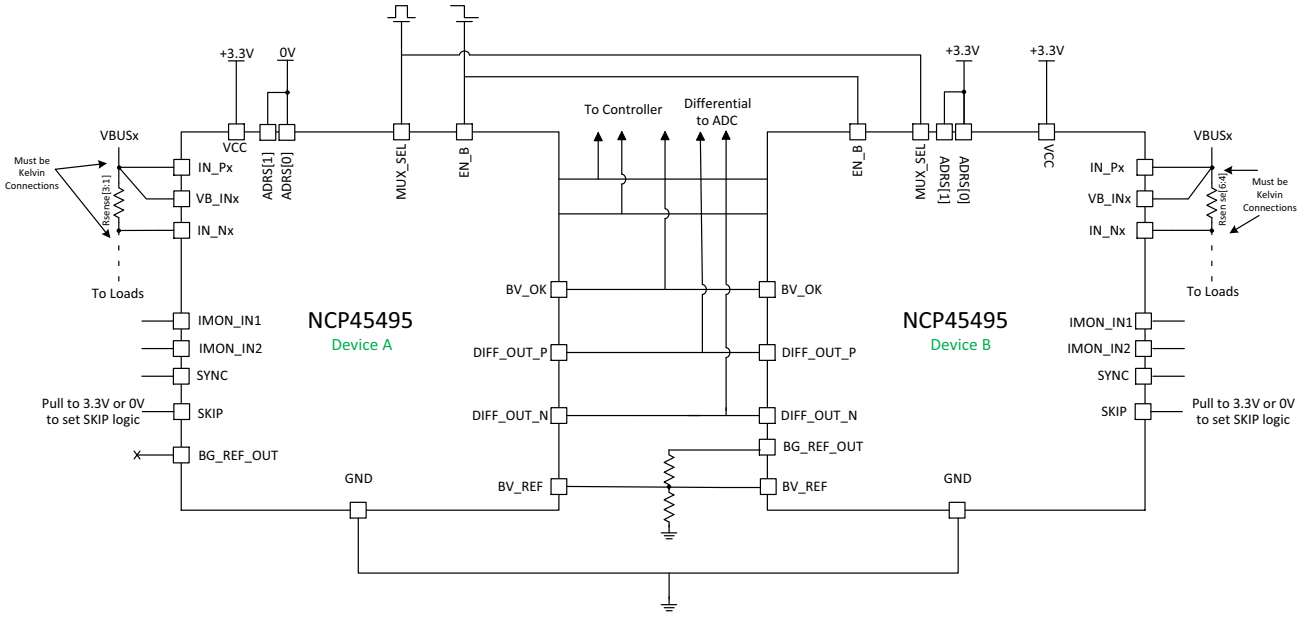


Figure 12. Six−Channel Paired Devices Connection Diagram

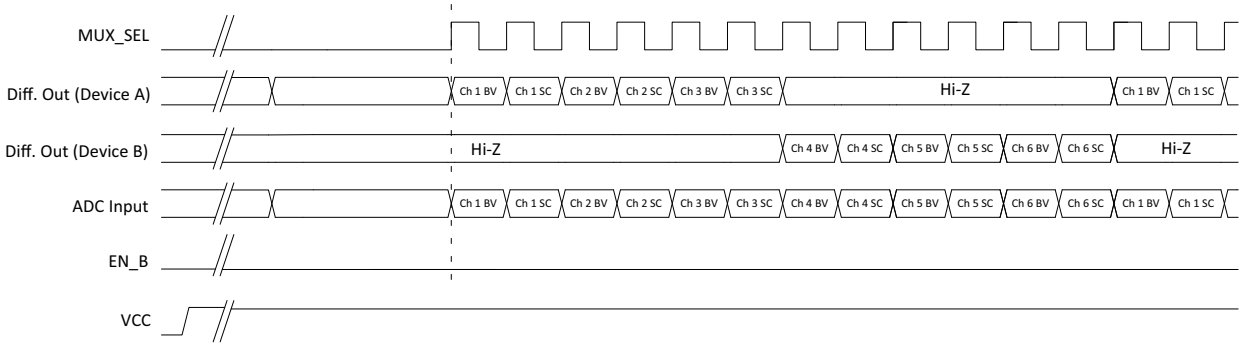


Figure 13. Six−Channel Paired Device Signal Characteristics with 6 Channels Activated

The following example shows the output sequence when all channels are active with a ground reference and alternating mode enabled in paired mode. The register settings for each device are shown below.

DEVICE A (I^2C address: 0x34)		DEVICE B (I^2C Address: 0x35)	
Register Address	Register Setting	Register Address	Register Setting
0x04	0xBF	0x04	0xBF
0x05	0x0B	0x05	0xB0
0x06	0x80	0x06	0x80

Clock Cycle	Diff Output (Device A)	Diff Output (Device B)
0	High Z	High Z
1	Ch 1 Bus Voltage	High Z
2	Ch 1 Shunt Current	High Z
3	Ch 2 Bus Voltage	High Z
4	Ch 2 Shunt Current	High Z
5	Ch 3 Bus Voltage	High Z
6	Ch 3 Shunt Current	High Z
7	Ch 4 Bus Voltage	High Z
8	Ch 4 Shunt Current	High Z
9	iMon1	High Z
10	iMon2	High Z
11	Ref GND	High Z
12	High Z	Ch 1 Bus Voltage
13	High Z	Ch 1 Shunt Current
14	High Z	Ch 2 Bus Voltage
15	High Z	Ch 2 Shunt Current
16	High Z	Ch 3 Bus Voltage
17	High Z	Ch 3 Shunt Current
18	High Z	Ch 4 Bus Voltage
19	High Z	Ch 4 Shunt Current
20	High Z	iMon1
21	High Z	iMon2
22	High Z	Ref GND
23	Ch 1 Bus Voltage Reversed	High Z
24	Ch 1 Shunt Current Reversed	High Z
25	Ch 2 Bus Voltage Reversed	High Z
26	Ch 2 Shunt Current Reversed	High Z
27	Ch 3 Bus Voltage Reversed	High Z
28	Ch 3 Shunt Current Reversed	High Z
29	Ch 4 Bus Voltage Reversed	High Z
30	Ch 4 Shunt Current Reversed	High Z
31	iMon1 Reversed	High Z
32	iMon2 Reversed	High Z
33	Ref GND Reversed	High Z
34	High Z	Ch 1 Bus Voltage Reversed
35	High Z	Ch 1 Shunt Current Reversed
36	High Z	Ch 2 Bus Voltage Reversed
37	High Z	Ch 2 Shunt Current Reversed
38	High Z	Ch 3 Bus Voltage Reversed
39	High Z	Ch 3 Shunt Current Reversed
40	High Z	Ch 4 Bus Voltage Reversed
41	High Z	Ch 4 Shunt Current Reversed
42	High Z	iMon1 Reversed
43	High Z	iMon2 Reversed
44	High Z	Ref GND Reversed
45	Ch 1 Bus Voltage	High Z

AUXILIARY FUNCTIONS

Bus Comparator (BV_OK): The BV_OK pin provides a real−time indication that V_{CC} and all bus voltages (as measured on the BV_INx pins) are valid. BV_OK remains low until all used BV_INx pins are above a user−defined threshold voltage. The BV_OK threshold is set by an external resistor divider on the BV_REF pin. The internal BV_OK comparator has built in hysteresis of 10% to prevent chatter as voltage busses come up. All channels specified in the ACTIVE_CHAN register will be represented. If desired, the user can use the SKIP pin to modify the logic as shown in the corresponding table (H = high, L = low, Z = tristate, X = don't care). The SKIP pin can also be used to hold BV_OK = L in the absence of V_{CC}.

VCC	EN_B	VB_INx	SKIP	BV_OK	Notes
L	L	X	L	open drain	No Power Provided to Part
L	L	X	H	L	SKIP Pin Provides Power Needed to Hold BV_OK Low
H	H	X	L	open drain	Standby Mode
H	H	X	H	L	Standby Mode
H	Z/L	L	H	L	Functional or Limited Mode
H	Z/L	H	H	open drain	Functional or Limited Mode
H	Z/L	X	L	open drain	Functional or Limited Mode

Reset/Timeout: If the timeout is enabled, holding the MUX_SEL pin HIGH or LOW linger then 45 μs will reset to the beginning of the MUX_SEL sequence. If the timeout has been disabled, then the MUX_SEL must cycle through all set channels to return to the beginning of the sequence. Toggling the EN_B pin will also reset the sequence back to the beginning.

Bandgap Reference: The BG_REF_OUT pin provides a high−accuracy voltage that can be used to generate the BV_REF voltage for the BV_OK comparators.

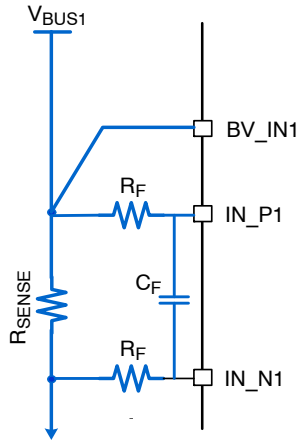
Enable Function: The EN_B pin controls device operation according to the corresponding table.

EN_B LOGIC

Level	Device Operation
LOW	Fully Functional
Tri−state (floating)	Limited Function: BG_REF_OUT is valid, BV_OK comparators and output are functional. All other functions to be disabled. DIFF_OUT to be Hi−Z and multiplexer select logic is held in reset.
HIGH	Standby: Power down state. Nothing is active.

Input Filtering:

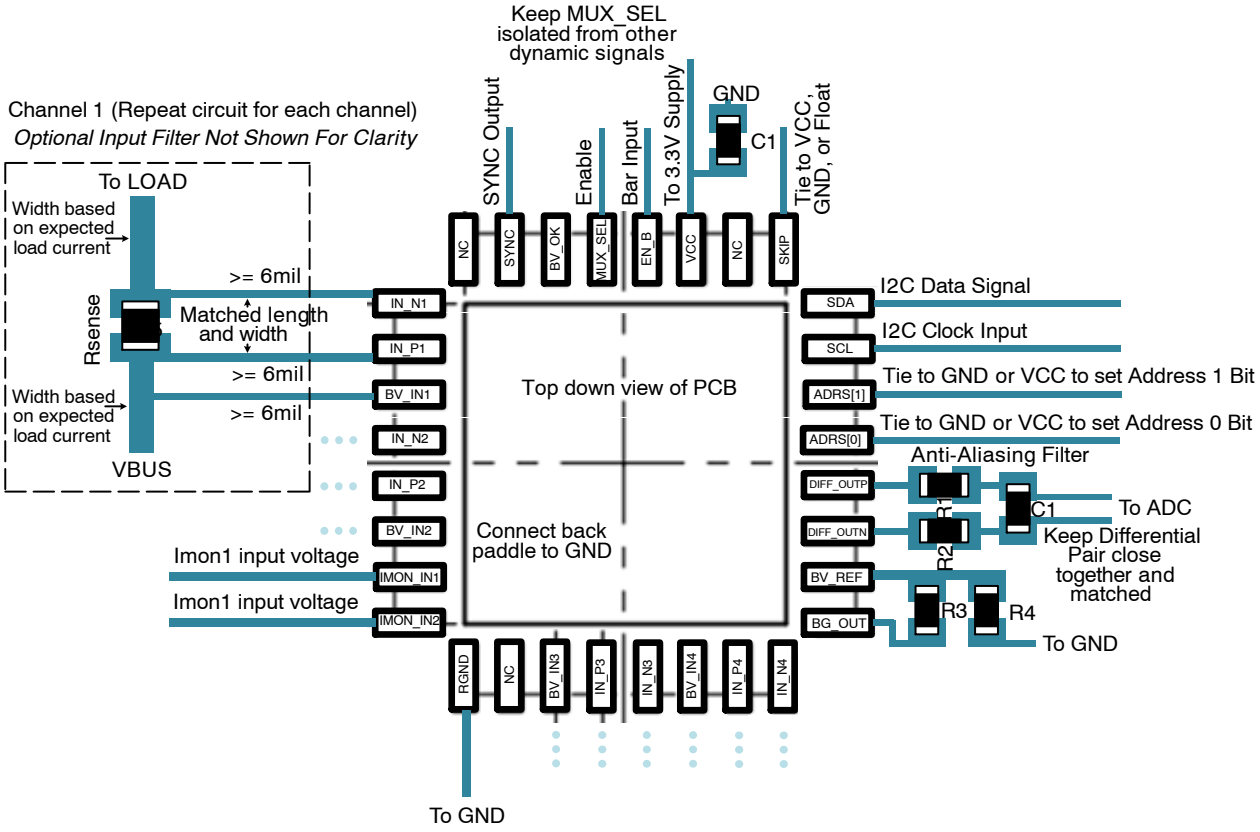
If additional filtering is needed on the input bus lines, external filtering can be added as shown below.



Mismatch between the 2 R_F values will contribute to the overall measurement offset error. To avoid this, the tolerance of external R_F resistors should be < 1%. External R_F values should not exceed 20 kΩ.

Layout Considerations

Sensitive signals that require special attention in board layout include the channel inputs (IN_N, IN_P, and BV_IN signals), the differential output signals, and the MUX_SEL signal. The IN_N and IN_P signals require a direct kelvin connection to the leads of the sense resistor to avoid parasitic trace resistance affecting the shunt current measurement. This direct connection is shown below. The sense resistors and connections from source to load for each channel need to be large enough to accommodate the expected high load currents.



Care should be taken to keep DIFF_OUT_P and DIFF_OUT_N matched. As a differential pair, any noise introduced to the pair will be common and will be rejected if the signals are close together and matched in length. Care should be taken to keep the MUX_SEL line isolated from other dynamically changing signals.

Unused Channels

Unused channels should be disabled by setting Register 0x04 over I^2C. The IN_P and IN_N pins for an unused channel should have the same connection. The following table details the recommended connections for unused pins.

Unused Pins	Connection
BV_INx	Connect to BV_IN pin of a previous channel or GND
IN_Px	Connect to the same potential as BV_INx or Float
IN_Nx	
IMONx	Float or GND
SYNC	Float

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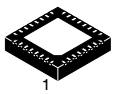
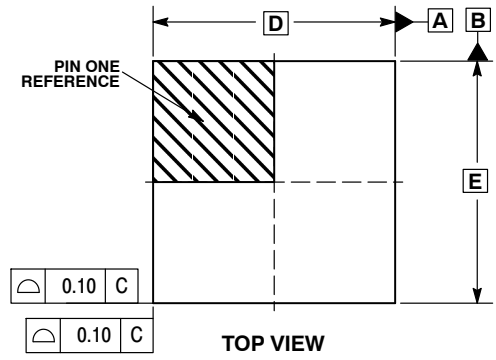
CASE 485CD
ISSUE A

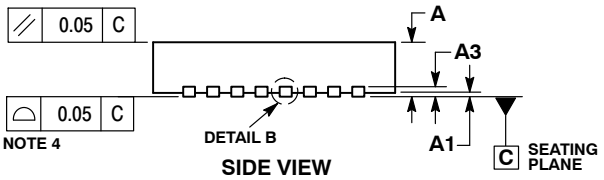
DATE 09 OCT 2012



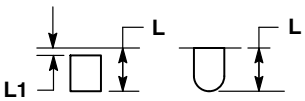
SCALE 2:1



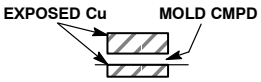
TOP VIEW



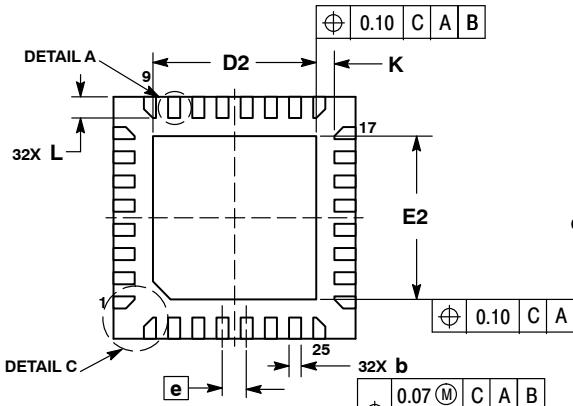
SIDE VIEW



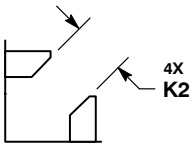
DETAIL A
ALTERNATE TERMINAL CONSTRUCTIONS



DETAIL B
ALTERNATE CONSTRUCTION



BOTTOM VIEW



DETAIL C
CORNER LEAD CONSTRUCTION

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.15	0.25
D	4.00 BSC	
D2	2.60	2.80
E	4.00 BSC	
E2	2.60	2.80
e	0.40 BSC	
K	0.30 REF	
K2	0.45 REF	
L	0.25	0.45
L1	---	0.15

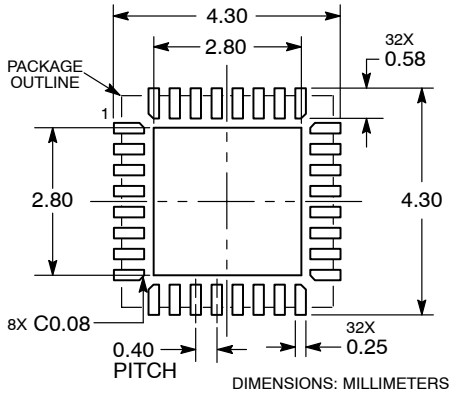
GENERIC MARKING DIAGRAM*

XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G”, may or not be present.

RECOMMENDED MOUNTING FOOTPRINT



DIMENSIONS: MILLIMETERS

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