NCP5380, NCP5380A

7-Bit, Programmable, Single-Phase, Synchronous Buck Switching Regulator Controller

ON Semiconductor®

http://onsemi.com

General Description

The NCP5380/A is a highly efficient, single−phase, synchronous buck switching regulator controller. With its integrated drivers, the NCP5380/A is optimized for converting the silver box voltage to the supply voltage required by high performance Intel chipsets. An internal 7−bit DAC is used to read a VID code directly from the chipset.

The NCP5380/A uses a multimode architecture. It provides programmable switching frequency that can be optimized for efficiency depending on the output current requirement. In addition, the NCP5380/A includes a programmable load line slope function to adjust the output voltage as a function of the load current so that the core voltage is always optimally positioned for a load transient. The NCP5380/A also provides accurate and reliable current overload protection and a delayed power−good output. The IC supports On−The−Fly (OTF) output voltage changes requested by the chipset.

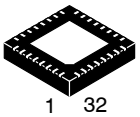
The NCP5380 is specified over the temperature range of 0°C to 85°C, while the NCP5380A extends the temperature range to −40°C to 100°C. The NCP5380/A is available in a 32−lead QFN.

Features

- Single−chip Solution
- Fully Compatible with the Intel VR11 CPU Chipset Voltage Regulator Specifications
- Integrated MOSFET Drivers
- ±8 mV Worst−case Differentially Sensed Core Voltage Error over Temperature
- Automatic Power−saving Modes Maximize Efficiency During Light Load Operation
- Soft Transient Control Reduces Inrush Current and Audio Noise
- Independent Current Limit and Load Line Setting Inputs for Additional Design Flexibility
- Built−in Power−good Masking Supports Voltage Identification (VID) OTF Transients
- 7−bit, Digitally Programmable DAC
- Short−circuit Protection with Programmable Latchoff Delay
- Current Monitor Output Signal
- 32−lead QFN
- This is a Pb−Free Device

Applications

- Desktop Power Supplies for Next−generation Intel Chipsets

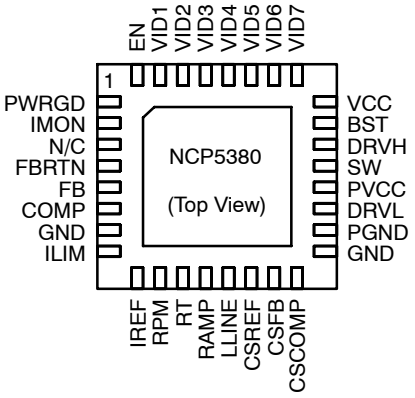


QFN32, 5x5
CASE 488AM
MN SUFFIX

MARKING DIAGRAM

NCP5380 = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
▪ = Pb Free Package
(Note: Microdot may be in either location)

PIN CONFIGURATION



ORDERING INFORMATION

Device	Package	Shipping†
NCP5380MNR2G	QFN−32 (Pb−Free)	5000 / Tape & Reel
NCP5380AMNR2G	QFN−32 (Pb−Free)	5000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

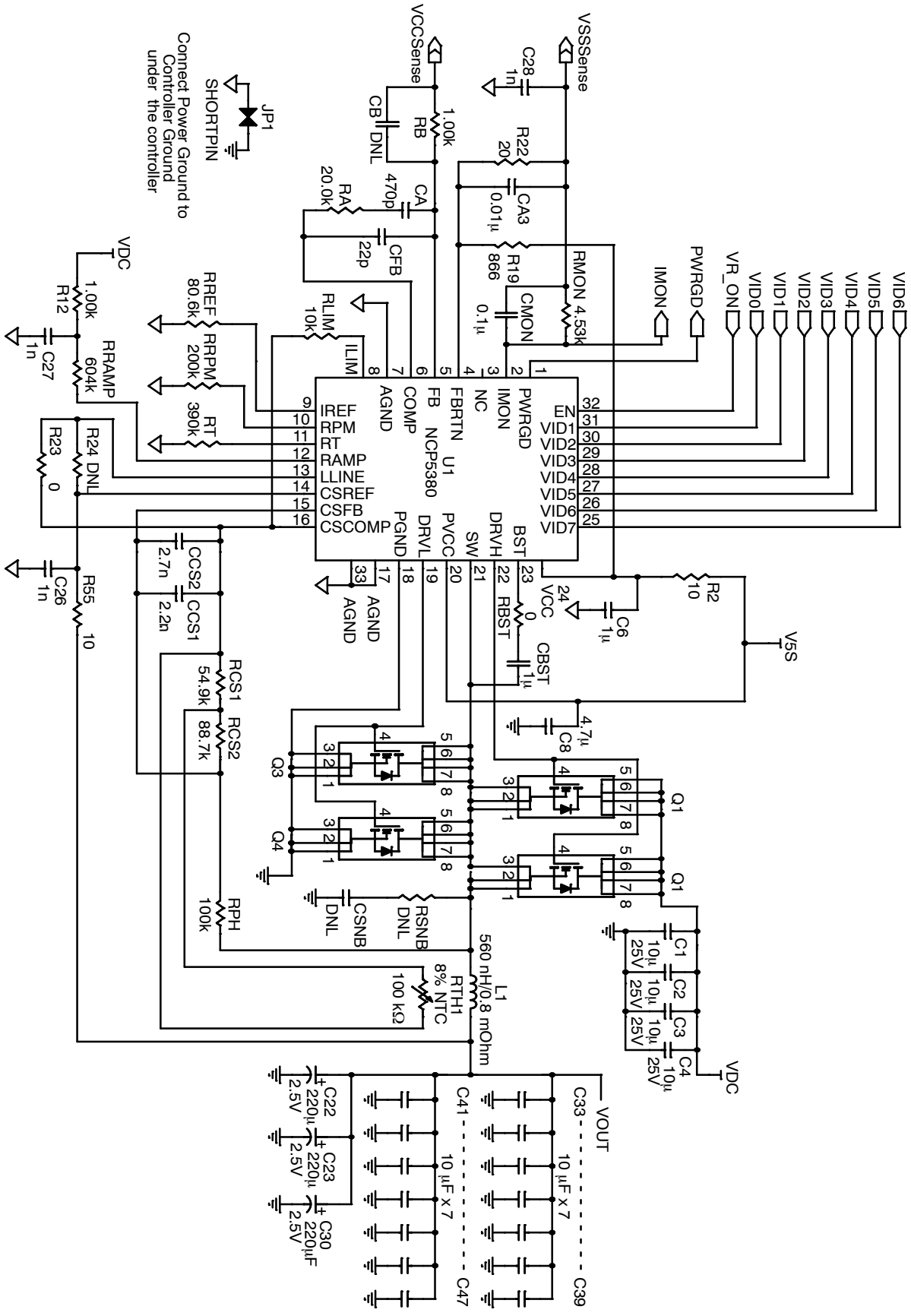


Figure 1. Application Schematic

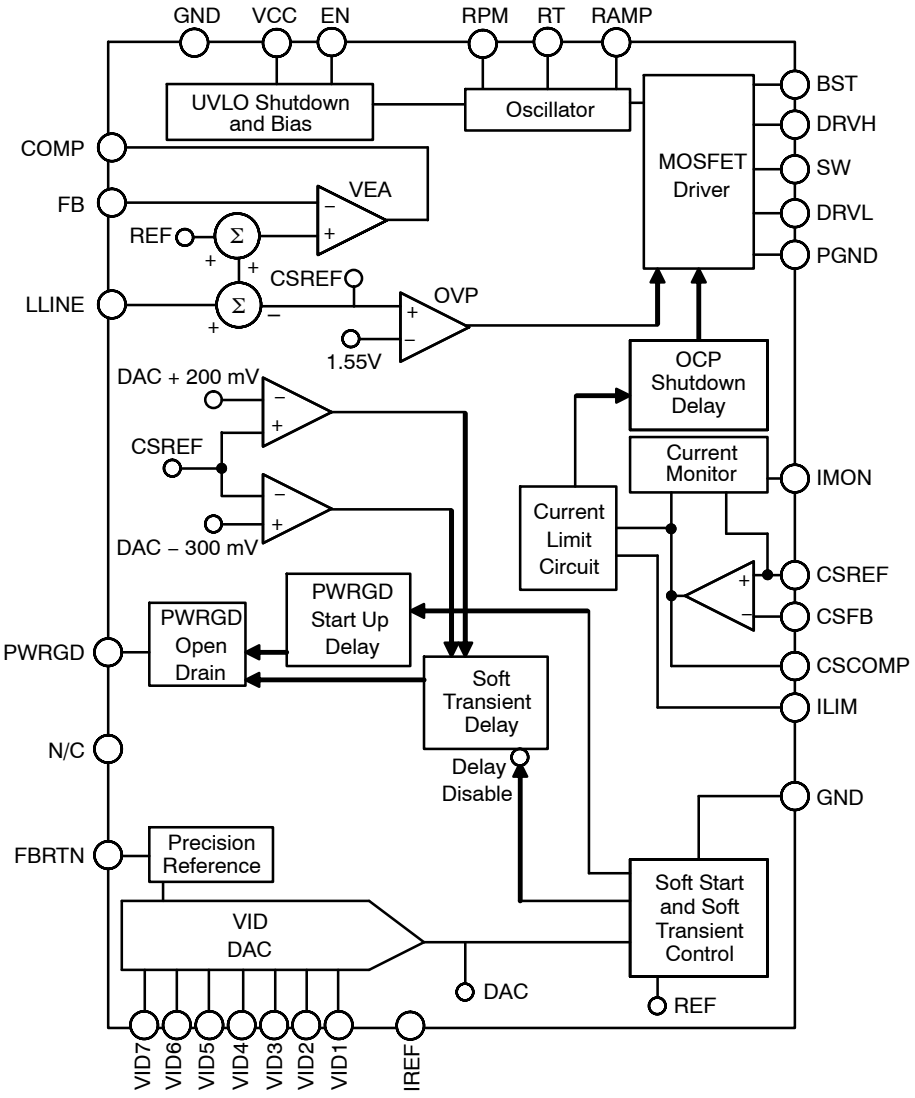


Figure 2. Functional Block Diagram

ELECTRICAL CHARACTERISTICS V_{CC} = 5.0 V, FBRTN = 112.5 mV, V_{VID} = 1.25 V, T_A = 0°C to 85°C (NCP5380), T_A = –40°C to 100°C (NCP5380A), unless otherwise noted (Note 1). Current entering a pin (sunk by the device) has a positive sign.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
VOLTAGE CONTROL VOLTAGE ERROR AMPLIFIER (VEAMP)						
FB, LLINE Voltage Range (Note 2)	V_{FB}, V_{LLINE}	Relative to CSREF = VDAC	–200		+200	mV
FB, LLINE Offset Voltage (Note 2)	V_{OSVEA}	Relative to CSREF = VDAC	–0.5		+0.5	mV
FB	I_{FB}		–1.0		+1.0	μA
LLINE Bias Current	I_{LLINE}		–10		+10	nA
LLINE Positioning Accuracy	V_{FB} – V_{DAC}	Measured on FB relative to nominal V_{DAC} –10°C to 100°C –40°C to 100°C	 –78 –77	 –80 –80	 –82 –83	mV
COMP Voltage Range	V_{COMP}	Voltage range of interest	0.85		4.0	V

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2. Guaranteed by design or bench characterization, not production tested.

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Parameter	Symbol	Conditions	Min	Typ	Max	Unit
VOLTAGE CONTROL VOLTAGE ERROR AMPLIFIER (VEAMP)						
COMP Current	I_{COMP}	COMP = 2.0 V, CSREF = VDAC FB forced 200 mV below CSREF FB forced 200 mV above CSREF		 −600 2.0		 μA mA
COMP Slew Rate	SR_{COMP}	C_{COMP} = 10 pF, CSREF = VDAC, Open loop configuration FB forced 200 mV below CSREF FB forced 200 mV above CSREF		 15 −20		V/μs
Gain Bandwidth (Note 2)	GBW	Non−inverting unit gain configuration, R_{FB} = 1 kΩ		20		MHz
VID DAC VOLTAGE REFERENCE						
VDAC Voltage Range (Note 2)		See VID table	0		1.6	V
VDAC Accuracy	V_{FB} − V_{DAC}	Measured on FB (includes offset), relative to nominal V_{DAC} V_{DAC} = 0.3 V to 1.2 V, −10°C to 100°C V_{DAC} = 0.3 V to 1.2 V, −40°C to 100°C V_{DAC} = 1.2125 V to 1.5 V, −40°C to 100°C	 −7.0 −9.0 −9.0		 +7.0 +9.0 +9.0	mV
VDAC Differential Nonlinearity (Note 2)			−1		+1	LSB
VDAC Line Regulation	ΔV_{FB}	VCC = 4.75 V to 5.25 V		0.05		%
VDAC Slew Rate		Soft−start Arbitrary VID step		0.0625 1		LSB/μs
FBRTN Current	I_{FBRTN}			70	200	μA
BOOT VOLTAGE						
Boot Voltage	V_{boot}			1.1		V
Boot Voltage Timer	t_{boot}		50	70	100	μs
VID DAC INPUTS						
Input Low Voltage	V_{IL}	VID(x)		0.5	0.3	V
Input High Voltage	V_{IH}	VID(x)	0.7	0.5		V
Input Current	$I_{IN(VID)}$	Sink current		1		μA
VID Transition Delay Time (Note 2)		VID Code Change to FB Change	400			ns
REFERENCE CURRENT						
I_{REF} Voltage	V_{IREF}	R_{IREF} = 80 kΩ to Set I_{REF} = 20 μA	1.55	1.6	1.65	μA
OSCILLATOR						
Frequency Range (Note 2)	f_{OSC}		0.3		3	MHz
Oscillator Frequency	F_{OSC}	T_A = +25°C, V_{VID} = 1.20 V, Clocked PWM Mode				kHz
		R_T = 60 kΩ	900	1200	1500	
		R_T = 120 kΩ	465	600	725	
		R_T = 180 kΩ	300	400	500	
RT Output Voltage	V_{RT}	V_{VID} = 1.6 V	1.08	1.2	1.35	V
RPM Output Current	I_{RPM}	V_{VID} = 1.250 V, R_T = 500 kΩ		−5		μA
RAMP Input Voltage	V_{RAMP}		0.9	1.0	1.1	V
RAMP Input Current Range	I_{RAMP}	EN = high	1		100	μA
RAMP Input Current in Shutdown		EN = low or in UVLO, RAMP = 19 V	−0.5		+0.5	μA

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Parameter	Symbol	Conditions	Min	Typ	Max	Unit
CURRENT SENSE AMPLIFIER						
Offset Voltage	$V_{OS(CSA)}$	CSFB − CSREF	−1.4		+1.4	mV
Input Bias Current	$I_{BIAS(CSFB)}$		−50		+50	nA
Gain Bandwidth Product (Note 2)	$GBW_{(CSA)}$			20		MHz
Slew Rate (Note 2)		C_{CSCOMP} = 10 pF		10		V/μs
Input Common−Mode Range (Note 2)		CSFB and CSREF	0		2	V
Output Voltage Range	V_{CSCOMP}		0.05		2	V
Output Current	I_{CSCOMP}	Source current		−650		μA
		Sink current		1		mA
SWITCH AMPLIFIER						
Common−Mode Range (Note 2)	V_{SW}		−400		+200	mV
Input Resistance	R_{SW}		0.8	1.5	2.0	kΩ
Zero Current Switching Threshold	$V_{ZCS(SW)}$	DCM Mode		−6		mV
DCM Minimum Off Time Masking	$t_{OFFMASK}$	SW falling		700		ns
CURRENT LIMIT COMPARATOR						
ILIM Voltage	V_{ILIM}− V_{CSCOMP}	R_{ILIMIT} = 5 kΩ, $V_{CSREF} - V_{CSCOMP}$ = 100 mV	−70	−100	−130	mV
	V_{ILIM}− V_{CSCOMP}	R_{ILIMIT} = 5 kΩ, $V_{CSREF} - V_{CSCOMP}$ = 0 mV	−1	0	1	mV
Current Limit Latch Off Delay		From OCP Event to PWRGD De−assertion		8		ms
SOFT−START						
Soft−Start Time	t_{ss}	From FB = 0V to FB = V_{boot}		1.4		ms
Soft−Start Delay		From EN POS Edge to FB = 50 mV		200		μs
SOFT TRANSIENT CONTROL						
Output Voltage Positive Slew Rate			10	12.5	15	mV/μs
Output Voltage Negative Slew Rate			−10	−12.5	−15	mV/μs
Extended PWRGD Masking Comparator Threshold	$V_{TH(ST)}$	|ST − V_{VID}|, ST falling		150		mV
SYSTEM LOGIC INPUTS						
Input Voltage	V_{EN}	Refers to driving signal level Logic low, I_{sink} = 1 μA			0.3	V
		Logic high, I_{source} = −5 μA	0.7			V
Input Current	I_{EN}	$V_{EN,VID[1:7]}$ = 0 V		10		nA
		0.2 V < $V_{EN,VID[1:7]}$ ≤ VCC		1		μA

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Parameter	Symbol	Conditions	Min	Typ	Max	Unit
POWER GOOD						
CSREF Undervoltage Threshold	$V_{UV(CSREF)}$	For VID = 1.2 V	−360	−300	−240	mV
CSREF Overvoltage Threshold	$V_{OV(CSREF)}$		150	200	250	mV
CSREF Crowbar (Overvoltage Protection) Threshold	$V_{CB(CSREF)}$	FBRTN = 112.5 mV	1.5	1.55	1.6	V
CSREF Reverse Voltage Detection Threshold	$V_{RVP(CSREF)}$	CSREF falling	−350	−300		mV
		CSREF rising		−75	−5	mV
PWRGD Output Low Voltage	$V_{OL(PWRGD)}$	$I_{SINK(PWRGD)}$ = 4 mA		75	100	mV
PWRGD Output Leakage Current		V_{PWRDG} = 3.3 V			0.5	μA
PWRGD Masking Time				100		μs
PWRGD delay Time	t_{PWRGD}		6	10	11	ms
CURRENT MONITOR						
IMON Output Current	I_{IMON}	$V_{CSREF} - V_{CSCOMP}$ = 100 mV	9	10	11	μA
IMON Output Current	I_{IMON}	$V_{CSREF} - V_{CSCOMP}$ = 10 mV	0.9	1	1.1	μA
IMON Clamp	V_{IMON}		1.0		1.15	V
HIGH−SIDE MOSFET DRIVER						
Output Resistance, Sourcing Current		BST − SW = 4.6 V		1.6	3.3	Ω
Output Resistance, Sinking Current		BST − SW = 4.6 V		1.3	2.8	Ω
Transition Times	$tr_{DRVH,}$	BST − SW = 4.6 V, C_L = 3 nF		15	35	ns
	tf_{DRVH}	BST − SW = 4.6 V, C_L = 3 nF		13	31	ns
Dead Delay Times	$tpdh_{DRVH}$	BST − SW = 4.6 V		20	45	ns
BST Quiescent Current		EN = low, shutdown		5	15	μA
		EN = high, no switching		200		μA
LOW−SIDE MOSFET DRIVER						
Output Resistance, Sourcing Current				1.4	3.0	Ω
Output Resistance, Sinking Current				1	2.7	Ω
Transition Times	tr_{DRVL}	C_L = 3 nF		15	35	ns
	tf_{DRVL}	C_L = 3 nF		14	35	ns
Propagation Delay Times	$tpdh_{DRVL}$	C_L = 3 nF		24	40	ns
SW Transition Timeout	$t_{TO(SW)}$	BST − SW = 4.6 V	150	250	450	ns
Zero−Crossing Threshold	V_{ZC}			1.5		V
PVCC Quiescent Current		EN = low, shutdown		14	50	μA
		EN = high, no switching		450		μA
BOOTSTRAP RECTIFIER						
Output Resistance			4.0	8.0	11	Ω
SOFT STOP						
CSREF Resistance to GND		EN = low or latch off		70		Ω

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Parameter	Symbol	Conditions	Min	Typ	Max	Unit
SUPPLY						
Supply Voltage Range (Note 2)		V_{CC}	4.5	5.5		V
Supply Current		Normal mode		4.2	10	mA
		EN = 0 V		60	200	μA
VCC OK Threshold Voltage	V_{CCOK}	VCC rising		4.4	4.5	V
VCC UVLO Threshold Voltage	V_{CCUVLO}	VCC falling	4.0	4.2		V
UVLO Hysteresis (Note 2)				250		mV

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Timing Diagram

Timing is referenced to the 90% and 10% points, unless otherwise noted.

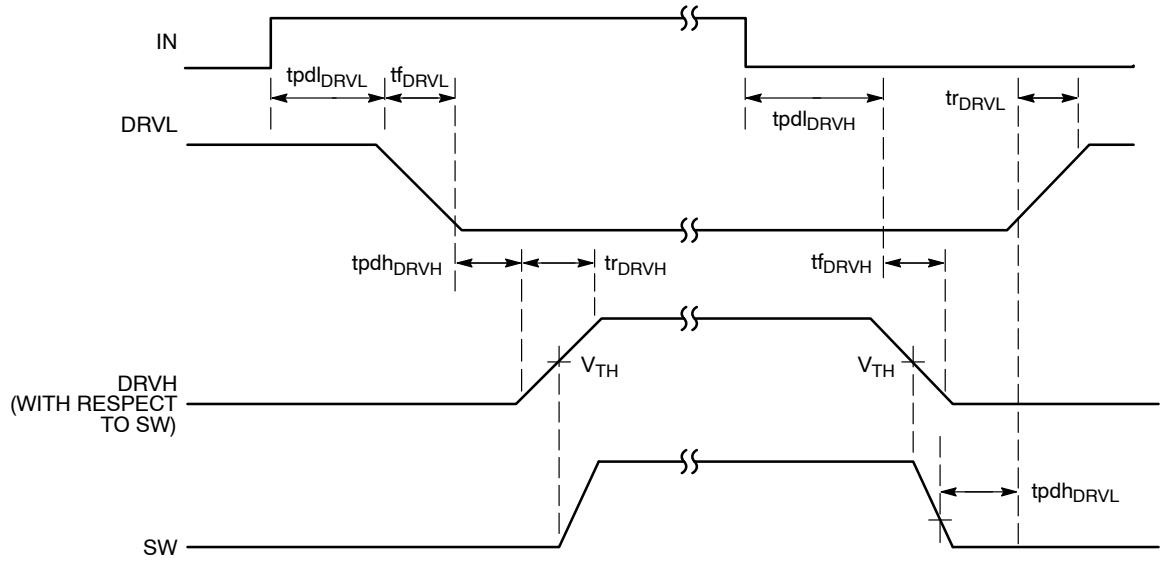


Figure 3. Timing Diagram

ABSOLUTE MAXIMUM RATING

Parameter		Rating
VCC		−0.3 V to +6.0 V
FBRTN, PGND		−0.3 V to +0.3 V
BST	DC	−0.3 V to +28 V
	t < 200 ns	−0.3 V to +33 V
BST to SW		−0.3 V to +6.0 V
DRVH, SW	DC	−5.0 V to +21 V
	t < 200 ns	−10 V to +26 V
DRVH to SW		−0.3 V to +6.0 V
DRVL to PGND	DC	−0.3 V to +6.0 V
	t < 200 ns	−5.0 V to +6.0 V
RAMP (in Shutdown)	DC	−0.3 V to +21 V
	t < 200 ns	−0.3 V to +26 V
All Other Inputs and Outputs		−0.3 V to +6.0 V
Storage Temperature		−65°C to +150°C
Operating Ambient Temperature Range		−40°C to 100°C
Operating Junction Temperature		125°C
Thermal Impedance (θ_{JA}) 2−Layer Board		32.6°C/W
Lead Temperature	Soldering (10 sec)	300°C
	Infrared (15 sec)	260°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Pin Function Descriptions

Pin No.	Mnemonic	Description
1	PWRGD	Power−Good Output. Open−drain output. A low logic state means that the output voltage is outside of the VID DAC defined range.
2	IMON	Current Monitor Output. This pin sources current proportional to the output load current. A resistor connected to VSS Sense sets the current monitor gain.
3	N/C	
4	FBRTN	Feedback Return Input/Output. This pin remotely senses the output voltage. It is also used as the ground return for the VID DAC and the voltage error amplifier blocks. It is also used to adjust the no−load offset.
5	FB	Voltage Error Amplifier Feedback Input. The inverting input of the voltage error amplifier.
6	COMP	Voltage Error Amplifier Output and Frequency Compensation Point.
7	GND	Analog and digital signal ground.
8	ILIM	Current Limit Set pin. Connect a resistor between ILIM and CSCOMP to the current limit threshold.
9	IREF	This pin sets the internal bias currents. A 100 kΩ is connected from IREF to ground.
10	RPM	RPM Mode Timing Control Input. A resistor is connected from RPM to ground sets the RPM mode turn−on threshold voltage.
11	RT	PWM Oscillator Frequency Setting Input. An external resistor from this pin to GND sets the PWM oscillator frequency.
12	RAMP	PWM Ramp Slope Setting Input. An external resistor from the converter input voltage node to this pin sets the slope of the internal PWM stabilizing ramp.
13	LLINE	Load Line Programming Input. The center point of a resistor divider connected between CSREF and CSCOMP tied to this pin sets the load line slope.
14	CSREF	Current Sense Reference Input. This pin must be connected to the opposite side of the output inductor.
15	CSFB	Noninverting Input of the Current Sense Amplifier. The combination of a resistor from the switch node to this pin and the feedback network from this pin to the CSCOMP pin sets the gain of the current sense amplifier.
16	CSCOMP	Current Sense Amplifier Output.
17	GND	Analog and Digital Signal Ground.
18	PGND	Low−Side Driver Power Ground. This pin should be connected close to the source of the lower MOSFET(s).
19	DRVL	Low−Side Gate Drive Output.
20	PVCC	Power Supply Input/Output of Low−Side Gate Driver.
21	SW	Current Return For High−Side Gate Drive.
22	DRVH	High−Side Gate Drive Output.
23	BST	High−Side Bootstrap Supply. A capacitor from this pin to SW holds the bootstrapped voltage while the high−side MOSFET is on.
24	VCC	Power Supply Input/Output of the Controller.
25 to 31	VID7 to VID1	Voltage Identification DAC Inputs. A 7−bit word (the VID code) programs the DAC output voltage, the reference voltage of the voltage error amplifier without a load (see the VID code table, Table 4). In normal operation mode, the VID DAC output programs the output voltage to a value within the 0 V to 1.6 V range (with FBRTN = 112.5 mV). The input is actively pulled down.
32	EN	Enable Input. Driving this pin low shuts down the chip, disables the driver outputs, and pulls PWRGD low.
Flag	PGND	High current power supply return via metal pad (flag) underneath package. Connect to pin 7.

Typical Performance Characteristics

V_{VID} = 1.5 V, T_A = 20°C to 100°C, unless otherwise noted.

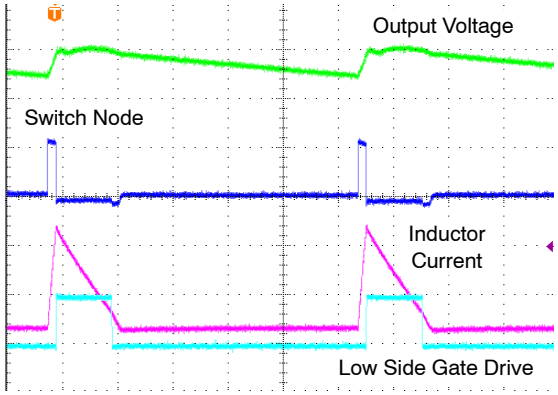


Figure 4. DCM Waveforms, 1 A Load Current

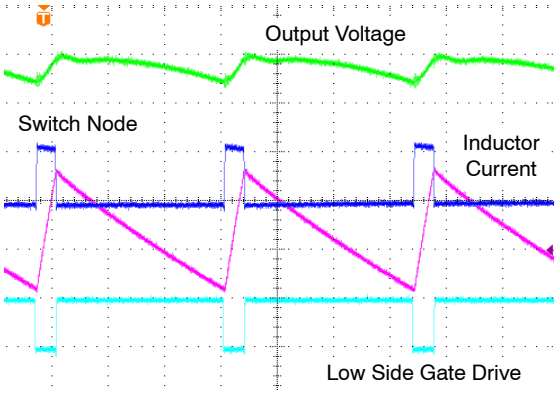


Figure 5. CCM Waveforms, 10 A Load Current

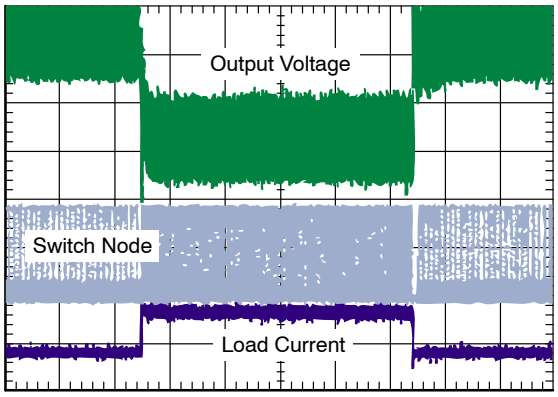


Figure 6. Load Transient, 2 A to 10 A, V_{IN} = 19 V

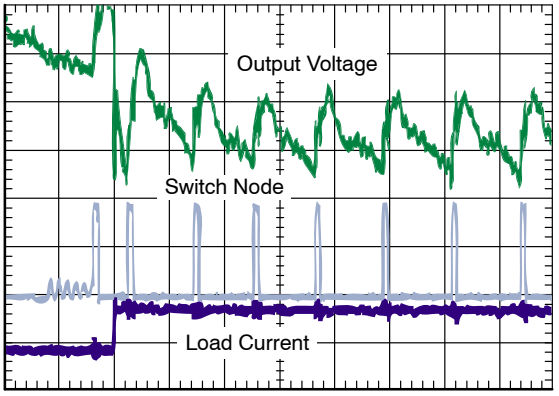


Figure 7. Load Transient, 2 A to 10 A, V_{IN} = 19 V

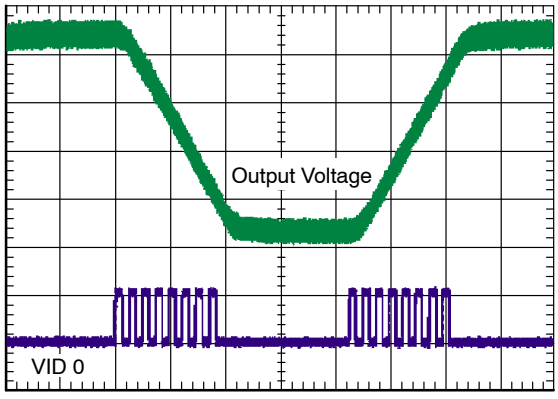


Figure 8. VID on the Fly, 1.25 V to 0.825 V

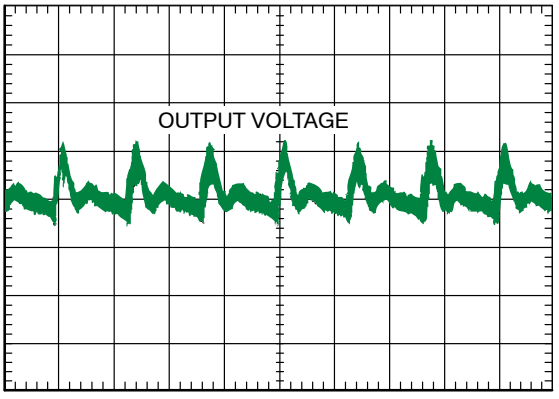


Figure 9. Output Ripple, 15 A Load, C_X = 470 μF, C_Z = 44 μF

Theory of Operation

The NCP5380/A is a ramp−pulse−modulated (RPM) controller for synchronous buck power supply. The internal 7−bit VID DAC conforms to the Intel VR11 specifications. The NCP5380/A is a stable, high performance architecture that includes

- High speed response at the lowest possible switching frequency and minimal count of output decoupling capacitors
- Minimized thermal switching losses due to lower frequency operation
- High accuracy load line regulation
- High power conversion efficiency with a light load by automatically switching to DCM operation

Operation Modes

The NCP5380/A runs in RPM mode for the purpose of fast transient response and high light load efficiency. During the following transients, the NCP5380/A runs in PWM mode:

- Soft−Start
- Soft transient: the period of 100 μs following any VID change
- Current overload

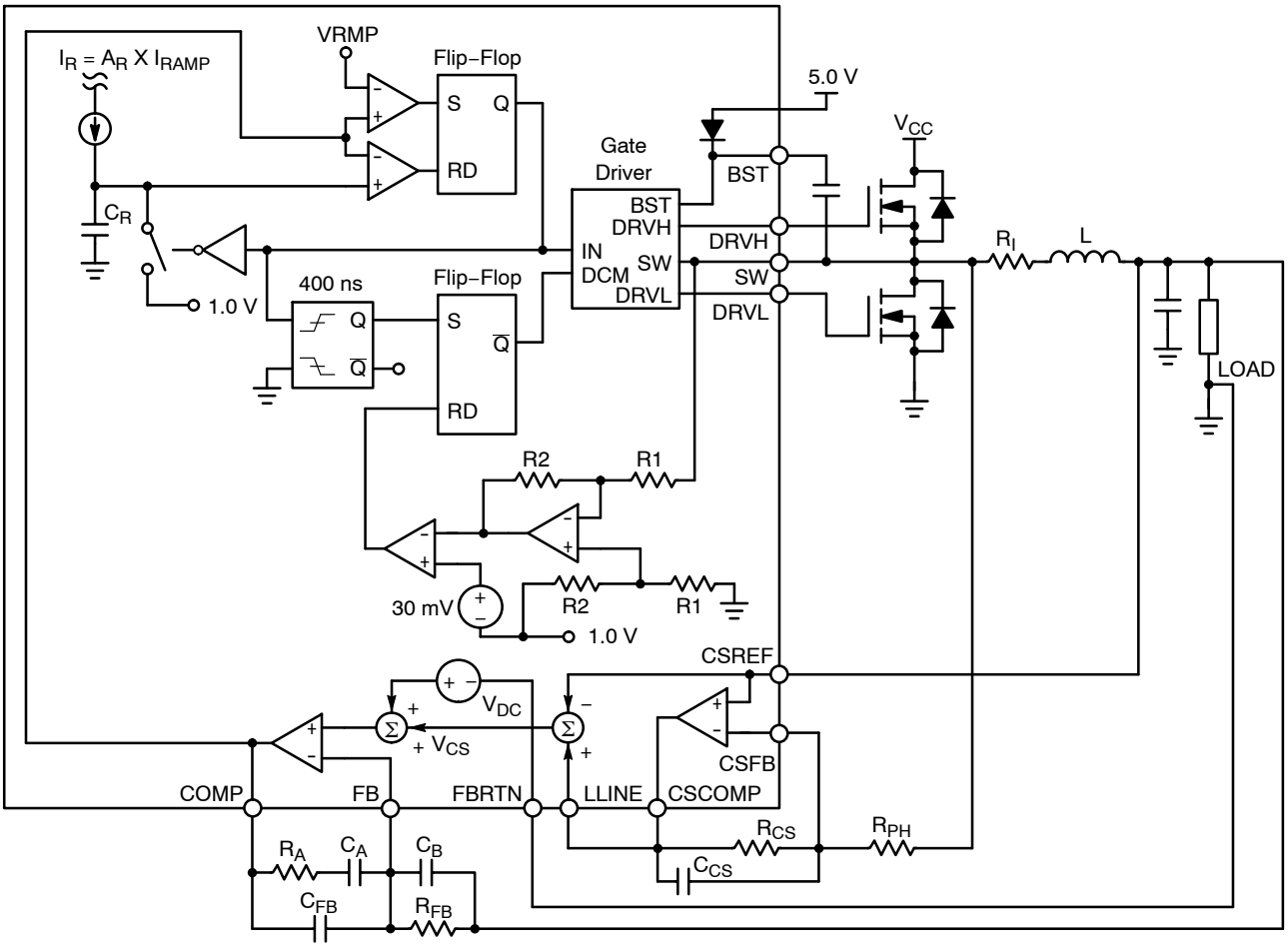


Figure 10. RPM Mode Operation

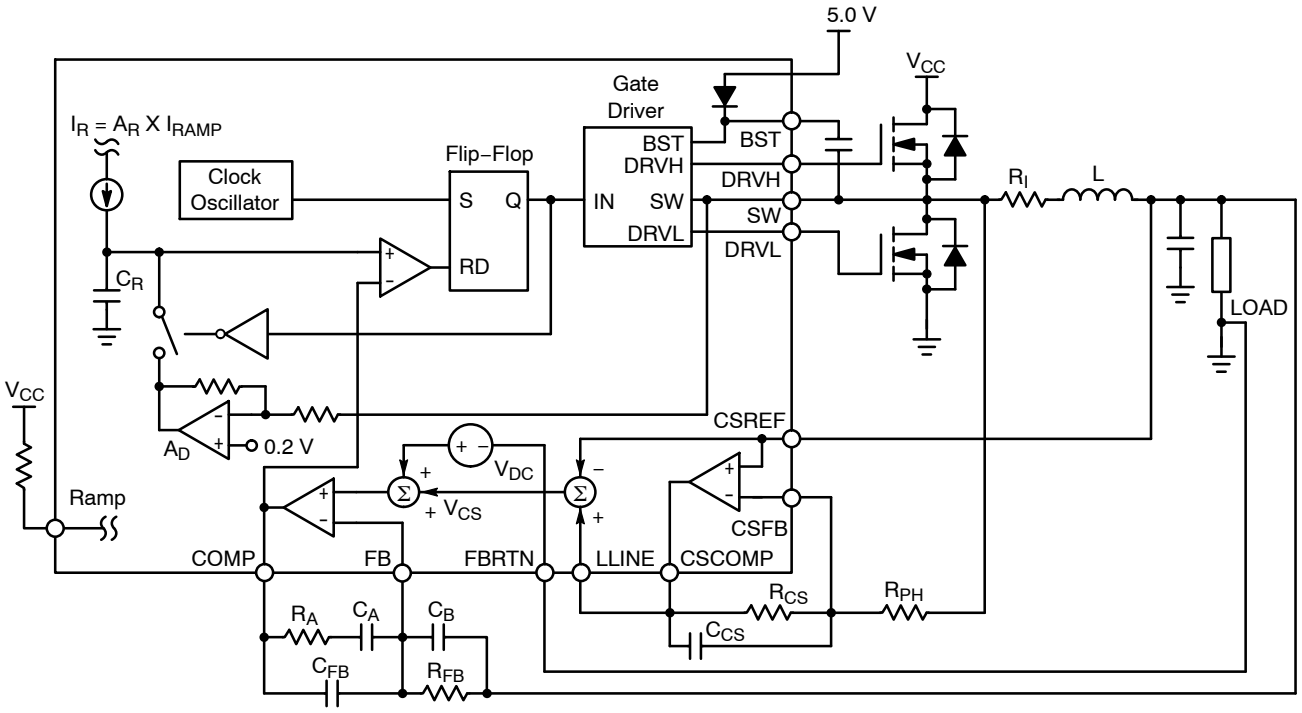


Figure 11. PWM Mode Operation

Setting Switch Frequency

Master Clock Frequency in PWM Mode

When the NCP5380/A runs in PWM, the clock frequency is set by an external resistor connected from the RT pin to GND. The frequency varies with the VID voltage: the lower the VID voltage, the lower the clock frequency. The variation of clock frequency with VID voltage maintains constant output ripple and improves power conversion efficiency at lower VID voltages.

Switching Frequency in RPM Mode

When the NCP5380/A operates in RPM mode, its switching frequency is controlled by the ripple voltage on the COMP pin. Each time the COMP pin voltage exceeds the RPM pin voltage threshold level determined by the VID voltage and the external resistor connected between RPM and ground, an internal ramp signal is started and DRVH is driven high. The slew rate of the internal ramp is programmed by the current entering the RAMP pin. One−third of the RAMP current charges an internal ramp capacitor (5 pF typical) and creates a ramp. When the internal ramp signal intercepts the COMP voltage, the DRVH pin is reset low.

In continuous current mode, the switching frequency of RPM operation is almost constant. While in discontinuous current conduction mode, the switching frequency is reduced as a function of the load current.

Differential Sensing of Output Voltage

The NCP5380/A combines differential sensing with a high accuracy VID DAC, referenced by a precision band gap source and a low offset error amplifier, In steady−state mode, the combination of the VID DAC and error amplifier maintain the output voltage for a worst−case scenario within ±8 mV of the full operating output voltage and temperature range.

The output voltage is sensed between the FB and FBRTN pins. FB should be connected through a resistor to the positive regulation point. FBRTN should be connected directly to the negative remote sensing point. The internal VID DAC and precision voltage reference are referenced to FBRTN thus allowing no load offset to be set using this pin.

Output Current Sensing

The NCP5380/A includes a dedicated current sense amplifier (CSA) to monitor the total output current of the converter for proper voltage positioning vs. load current and for overcurrent detection. Sensing the current delivered to the load is an inherently more accurate method than detecting peak current or sampling the current across a sense element, such as the low−side MOSFET. The current sense amplifier can be configured several ways, depending on system optimization objectives, and the current information can be obtained by

- Output inductor ESR sensing without the use of a thermistor for the lowest cost
- Output inductor ESR sensing with the use of a thermistor that tracks inductor temperature to improve accuracy
- Discrete resistor sensing for the highest accuracy

At the positive input of the CSA, the CSREF pin is connected to the output voltage. At the negative input (that

is, the CSFB pin of the CSA), signals from the sensing element (in the case of inductor DCR sensing, signals from the switch node side of the output inductors) are connected with a resistor. The feedback resistor between the CSCOMP and CSFB pins sets the gain of the current sense amplifier, and a filter capacitor is placed in parallel with this resistor. The current information is then given as the voltage difference between the CSCOMP and CSREF pins. This signal is used internally as a differential input for the current limit comparator.

An additional resistor divider connected between the CSCOMP and CSREF pins with the midpoint connected to the LLINE pin can be used to set the load line. The current information to set the load line is then given as the voltage difference between the LLINE and CSREF pins. This configuration allows the load line slope to be set independent from the current limit threshold. If the current limit threshold and load line do not have to be set independently, the resistor divider between the CSCOMP and CSREF pins can be omitted and the CSCOMP pin can be connected directly to LLINE. To disable voltage positioning entirely (that is, to set no load line), LLINE should be tied to CSREF.

To provide the best accuracy for current sensing, the CSA has a low offset input voltage and the sensing gain is set by an external resistor ratio.

Active Impedance Control Mode

To control the dynamic output voltage droop as a function of the output current, the signal that is proportional to the total output current, converted from the voltage difference between LLINE and CSREF, can be scaled to be equal to the required droop voltage. This droop voltage is calculated by multiplying the droop impedance of the regulator by the output current. This value is used as the control voltage of the PWM regulator. The droop voltage is subtracted from the DAC reference output voltage, and the resulting voltage is used as the voltage positioning setpoint. The arrangement results in an enhanced feedforward response.

Voltage Control Mode

A high−gain bandwidth error amplifier is used for the voltage mode control loop. The noninverting input voltage is set via the 7−bit VID DAC. The noninverting input voltage is offset by the droop voltage as a function of current, commonly known as active voltage positioning. The output of the error amplifier is the COMP pin, which sets the termination voltage of the internal PWM ramps.

At the negative input, the FB pin is tied to the output sense location using R_B, a resistor for sensing and controlling the output voltage at the remote sensing point. The main loop compensation is incorporated in the feedback network connected between the FB and COMP pins.

Power−Good Monitoring

The power−good comparator monitors the output voltage via the CSREF pin. The PWRGD pin is an open−drain output that can be pulled up through an external resistor to a voltage rail − not necessarily the same VCC voltage rail that is running the controller. A logic high level indicates that the output voltage is within the voltage limits defined by a range around the VID voltage setting. PWRGD goes low when the output voltage is outside of this range.

Following the CPU specification, the PWRGD range is defined to be 300 mV less than and 200 mV greater than the actual VID DAC output voltage. To prevent a false alarm, the power−good circuit is masked during any VID change and during soft−start. The duration of the PWRGD mask is set to approximately 100 μs by an internal timer. In addition, for a VID change from high to low, there is an additional period of PWRGD masking before the internal DAC voltage drops within 200 mV of the new lower VID DAC output voltage, as shown in Figure 12.

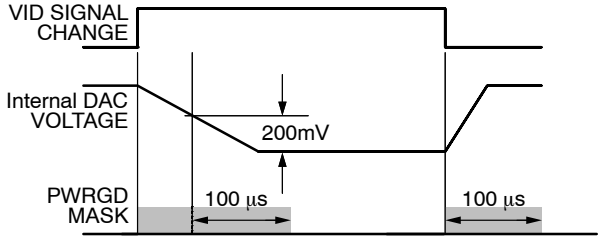


Figure 12. PWRGD Masking for VID Change

Power−Up Sequence and Soft−Start

The power−on ramp−up time of the output voltage is set internally. The power−up sequence is illustrated in Figure 13.

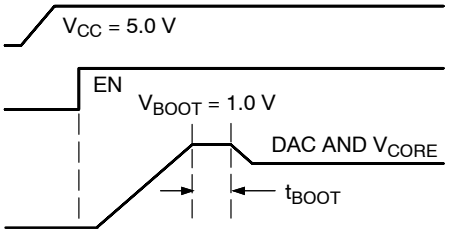


Figure 13. Power−Up Sequence for CPU

VID Change and Soft Transient

When a VID input changes, the NCP5380/A detects the change but ignores new code for a minimum of 400 ns. This delay is required to prevent the device from reacting to digital signal skew while the 7−bit VID input code is in transition. Additionally, the VID change triggers a PWRGD masking timer to prevent a PWRGD failure. Each VID change resets and retriggers the internal PWRGD masking timer.

The NCP5380/A provides a soft transient function to reduce inrush current during VID transitions. Reducing the inrush current helps decrease the acoustic noise generated by the MLCC input capacitors and inductors.

The soft transient feature is implemented internally. When a new VID code is detected, the NCP5380/A steps

sequentially through each VID voltage to the final VID voltage.

Current Limit, Short−Circuit, and Latchoff Protection

The NCP5380/A has an adjustable current limit set by the R_{CLIM} resistor. The NCP5380/A compares a programmable current−limit set point to the voltage from the output of the current−sense amplifier. The level of current limit is set with the resistor from the ILIM pin to CSCOMP. During operation, the voltage on ILIM is equal to the voltage on CSREF. The current through the external resistor connected between ILIM and CSCOMP is then compared to the internal current limit current I_{cl}. If the current generated through this resistor into the ILIM pin(Ilim) exceeds the internal current−limit threshold current (I_{cl}), the internal current−limit amplifier controls the internal COMP voltage to maintain the average output current at the limit.

Normally, the NCP5380/A operates in RPM mode. During a current overload, the NCP5380/A switches to PWM mode.

With low impedance loads, the NCP5380/A operates in a constant current mode to ensure that the external MOSFETs and inductor function properly and to protect the CPU. With a low constant impedance load, the output voltage decreases to supply only the set current limit. If the output voltage drops below the power−good limit, the PWRGD signal transitions. After the PWRGD single transitions, internal waits 7 ms before latching off the NCP5380/A.

Figure 14 shows how the NCP5380/A reacts to a current overload.

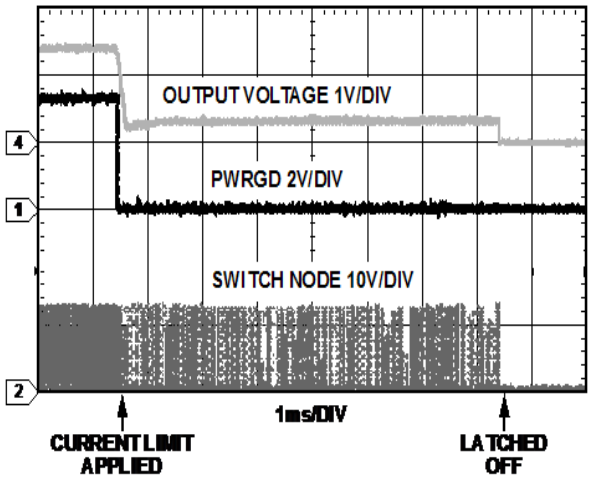


Figure 14. Current Overload

The latchoff function can be reset either by removing and reapplying VCC or by briefly pulling the EN pin low.

During startup, when the output voltage is below 200 mV, a secondary current limit is active. This is necessary because the voltage swing of CSCOMP cannot extend below ground. This secondary current limit clamp controls the minimum internal COMP voltage to the PWM comparators to 1.5 V. This limits the voltage drop across the low−side MOSFETs through the current balance circuitry.

Light Load RPM DCM Operation

The NCP5380/A operates in RPM mode. With higher loads, the NCP5380/A operates in continuous conduction mode (CCM), and the upper and lower MOSFETs run synchronously and in complementary phase. See Figure 15 for the typical waveforms of the NCP5380/A running in CCM with a 7 A load current.

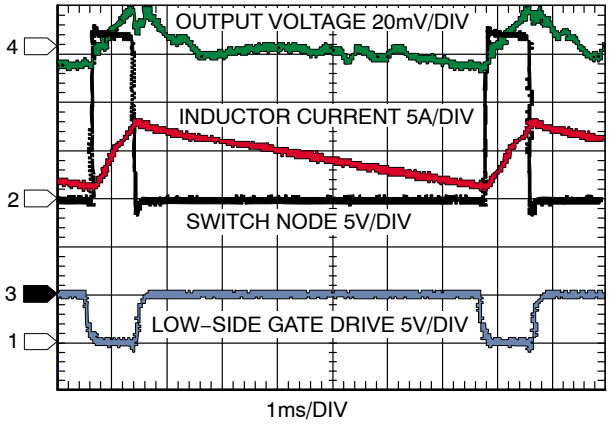


Figure 15. Single−Phase Waveforms in CCM

With lighter loads, the NCP5380/A enters discontinuous conduction mode (DCM). Figure 16 shows a typical single-phase buck with one upper FET, one lower FET, an output inductor, an output capacitor, and a load resistor. Figure 17 shows the path of the inductor current with the upper FET on and the lower FET off. In Figure 18 the high-side FET is off and the low-side FET is on. In CCM, if one FET is on, its complementary FET must be off; however, in DCM, both high- and low-side FETs are off and no current flows into the inductor (see Figure 19). Figure 20 shows the inductor current and switch node voltage in DCM.

In DCM with a light load, the NCP5380/A monitors the switch node voltage to determine when to turn off the low-side FET. Figure 20 shows a typical waveform in DCM with a 1 A load current. Between t1 and t2, the inductor current ramps down. The current flows through the source drain of the low-side FET and creates a voltage drop across the FET with a slightly negative switch node. As the inductor current ramps down to 0 A, the switch voltage approaches 0 V, as seen just before t2. When the switch voltage is approximately −6 mV, the low-side FET is turned off.

Figure 20 shows a small, dampened ringing at t2. This is caused by the LC created from capacitance on the switch node, including the CDS of the FETs and the output inductor. This ringing is normal.

The NCP5380/A automatically goes into DCM with a light load. Figure 21 shows the typical DCM waveform of the NCP5380/A with a 1 A load current. As the load increases, the NCP5380/A enters into CCM. In DCM, frequency decreases with load current, and switching frequency is a function of the inductor, load current, input voltage, and output voltage.

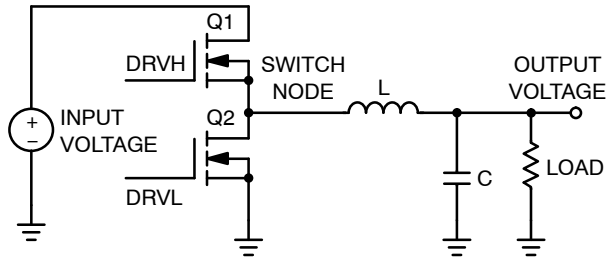


Figure 16. Buck Topology

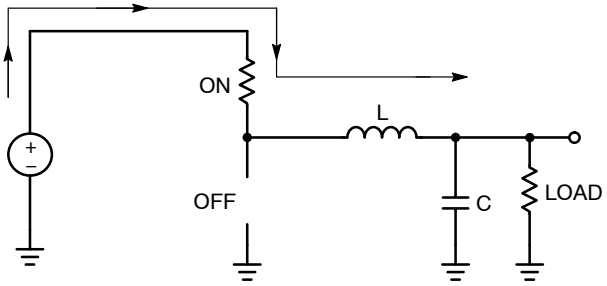


Figure 17. Buck Topology Inductor Current During t_0 and t_1

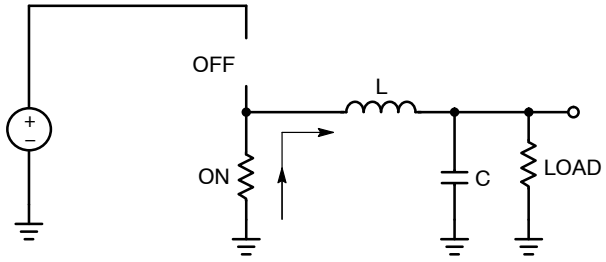


Figure 18. Buck Topology Inductor Current During t_1 and t_2

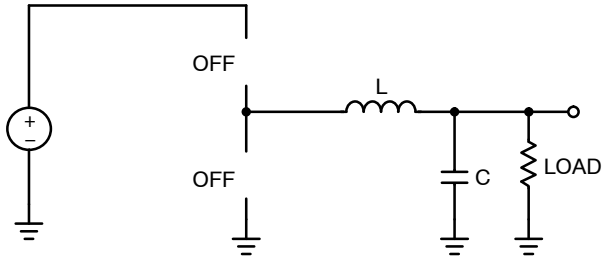


Figure 19. Buck Topology Inductor Current During t_2 and t_3

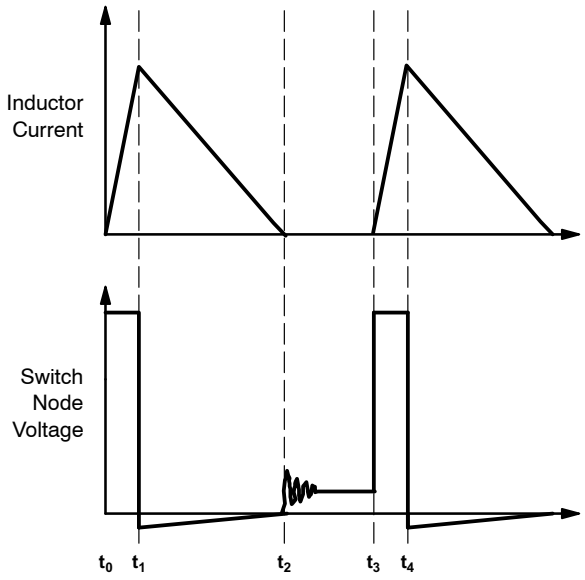


Figure 20. Inductor Current and Switch Node in DCM

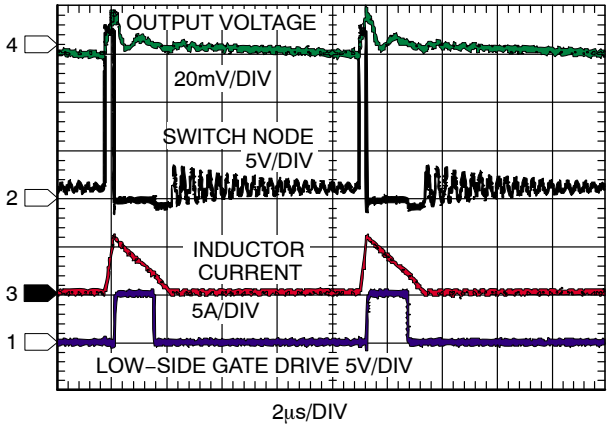


Figure 21. Single−Phase Waveforms in DCM with 1 A Load Current

Output Crowbar

To protect the load and output components of the supply, the DRVL output is driven high (turning the low−side MOSFETs on) and DRVH is driven low (turning the high−side MOSFETs off) when the output voltage exceeds the CPU OVP threshold.

Turning on the low−side MOSFETs forces the output capacitor to discharge and the current to reverse due to current build up in the inductors. If the output overvoltage is due to a drain−source short of the high−side MOSFET, turning on the low−side MOSFET results in a crowbar across the input voltage rail. The crowbar action blows the fuse of the input rail, breaking the circuit and thus protecting the CPU chipset from destruction.

When the OVP feature is triggered, the NCP5380 is latched off. The latchoff function can be reset by removing and reapplying VCC to the NCP5380/A or by briefly pulling the EN pin low.

Reverse Voltage Protection

Very large reverse current in inductors can cause negative output voltage, which is harmful to the chipset and other output components. The NCP5380/A provides a reverse voltage protection (RVP) function without additional system cost. The output voltage is monitored through the CSREF pin. When the CSREF pin voltage drops to less than −190 mV, the NCP5380/A triggers the RVP function by setting both DRVH and DRVL low, thus turning off all MOSFETs. The reverse inductor currents can be quickly reset to 0 by discharging the built−up energy in the inductor into the input dc voltage source via the forward−biased body diode of the high−side MOSFETs. The RVP function is terminated when the CSREF pin voltage returns to greater than −150 mV.

Sometimes the crowbar feature inadvertently results in negative voltage because turning on the low−side MOSFETs results in a very large reverse inductor current. To prevent damage to the chipset caused from negative voltage, the NCP5380/A maintains its RVP monitoring function even after OVP latchoff. During OVP latchoff, if the CSREF pin voltage drops to less than −190 mV, the low−side MOSFETs is turned off by setting DRVL low. DRVL will be set high again when the CSREF voltage recovers to greater than +50 mV.

Figure 22 shows the reverse voltage protection function of the NCP5380/A. The CSREF pin is disconnected from the output voltage and pulled negative. As the CSREF pin drops to less than −190 mV, the low−side and high−side FETs turn off.

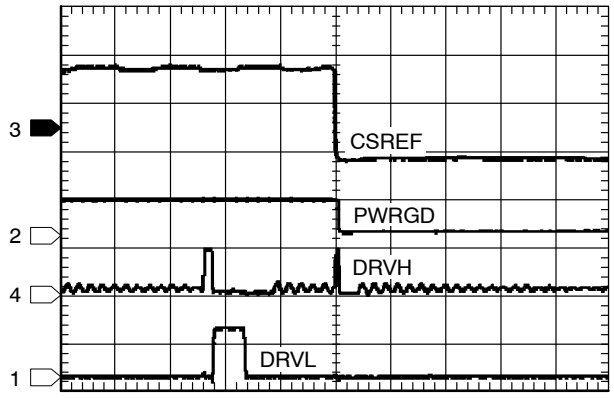


Figure 22. NCP5380 RVP Function

Output Enable and UVLO

For the NCP5380/A to begin switching, the V_{CC} supply voltage to the controller must be greater than the V_{CCOK} threshold and the EN pin must be driven high. If the V_{CC} voltage is less than the V_{CCUVLO} threshold or the EN pin is logic low, the NCP5380/A shuts off. In shutdown mode, the controller holds DRVH and DRVL low, shorts the capacitors of the SS and PGDELAY pins to ground, and drives PWRGD to low.

The user must adhere to proper power−supply sequencing during startup and shutdown of the NCP5380/A. All input pins must be at ground prior to removing or applying V_{CC}, and all output pins should be left in high impedance state while V_{CC} is off.

Output Current Monitor

The NCP5380/A includes an output current monitor function. The IMON pin outputs an accurate current that is directly proportional to the output current. This current is then run through a parallel RC connected from the IMON pin to the FBRTN pin to generate an accurately scaled and filtered voltage. The maximum voltage on IMON is internally clamoed by the NCP5380/A at 1.15 V.

Output Voltage No-load Offset Adjustment

The NCP5380/A output voltage can be offset from the nominal VID settings by adjusting one resistor value. The following figure shows the components used for setting the no-load output offset voltage.

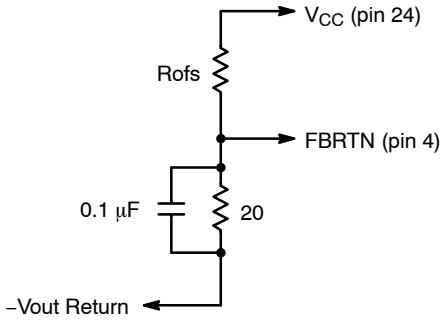


Figure 23. Setting the Output Offset Voltage

The nominal VID table for the NCP5380/A is based on the voltage at FBRTN being 112.5 mV (R_{ofs} nominal of 866 ohms). If it is desired to adjust the no-load output voltage to be above or below VID, then the value of R_{ofs} can be changed. If we define the no-load offset from VID as V_{nlofs}, then the following can be used to determine the value for R_{ofs} (given V_{CC} = 5 V);

$$R_{ofs} = \left(\frac{5}{0.1125 + V_{nlofs}} - 1\right) \times 20$$

NOTE: The 20 ohm resistor and 0.1 μF capacitor nominal values are fixed based on the design of the NCP5380/A so only R_{ofs} should be adjusted for changing the no−load offset.

VID Codes (FBRTN = 112.5 mV)

VID7	VID6	VID5	VID4	VID3	VID2	VID1	Output
0	0	0	0	0	0	1	1.6000
0	0	0	0	0	1	0	1.5875
0	0	0	0	0	1	1	1.5750
0	0	0	0	1	0	0	1.5625
0	0	0	0	1	0	1	1.5500
0	0	0	0	1	1	0	1.5375
0	0	0	0	1	1	1	1.5250
0	0	0	1	0	0	0	1.5125
0	0	0	1	0	0	1	1.5000
0	0	0	1	0	1	0	1.4875
0	0	0	1	0	1	1	1.4750
0	0	0	1	1	0	0	1.4625
0	0	0	1	1	0	1	1.4500
0	0	0	1	1	1	0	1.4375
0	0	0	1	1	1	1	1.4250
0	0	1	0	0	0	0	1.4125
0	0	1	0	0	0	1	1.4000
0	0	1	0	0	1	0	1.3875
0	0	1	0	0	1	1	1.3750
0	0	1	0	1	0	0	1.3625
0	0	1	0	1	0	1	1.3500
0	0	1	0	1	1	0	1.3375
0	0	1	0	1	1	1	1.3250
0	0	1	1	0	0	0	1.3125
0	0	1	1	0	0	1	1.3000
0	0	1	1	0	1	0	1.2875
0	0	1	1	0	1	1	1.2750
0	0	1	1	1	0	0	1.2625
0	0	1	1	1	0	1	1.2500
0	0	1	1	1	1	0	1.2375
0	0	1	1	1	1	1	1.2250
0	1	0	0	0	0	0	1.2125
0	1	0	0	0	0	1	1.2000
0	1	0	0	0	1	0	1.1875
0	1	0	0	0	1	1	1.1750
0	1	0	0	1	0	0	1.1625
0	1	0	0	1	0	1	1.1500
0	1	0	0	1	1	0	1.1375
0	1	0	0	1	1	1	1.1250
0	1	0	1	0	0	0	1.1125
0	1	0	1	0	0	1	1.1000
0	1	0	1	0	1	0	1.0875
0	1	0	1	0	1	1	1.0750
0	1	0	1	1	0	0	1.0625
0	1	0	1	1	0	1	1.0500

VID Codes (FBRTN = 112.5 mV)

VID7	VID6	VID5	VID4	VID3	VID2	VID1	Output
0	1	0	1	1	1	0	1.0375
0	1	0	1	1	1	1	1.0250
0	1	1	0	0	0	0	1.0125
0	1	1	0	0	0	1	1.0000
0	1	1	0	0	1	0	0.9875
0	1	1	0	0	1	1	0.9750
0	1	1	0	1	0	0	0.9625
0	1	1	0	1	0	1	0.9500
0	1	1	0	1	1	0	0.9375
0	1	1	0	1	1	1	0.9250
0	1	1	1	0	0	0	0.9125
0	1	1	1	0	0	1	0.9000
0	1	1	1	0	1	0	0.8875
0	1	1	1	0	1	1	0.8750
0	1	1	1	1	0	0	0.8625
0	1	1	1	1	0	1	0.8500
0	1	1	1	1	1	0	0.8375
0	1	1	1	1	1	1	0.8250
1	0	0	0	0	0	0	0.8125
1	0	0	0	0	0	1	0.8000
1	0	0	0	0	1	0	0.7875
1	0	0	0	0	1	1	0.7750
1	0	0	0	1	0	0	0.7625
1	0	0	0	1	0	1	0.7500
1	0	0	0	1	1	0	0.7375
1	0	0	0	1	1	1	0.7250
1	0	0	1	0	0	0	0.7125
1	0	0	1	0	0	1	0.7000
1	0	0	1	0	1	0	0.6875
1	0	0	1	0	1	1	0.6750
1	0	0	1	1	0	0	0.6625
1	0	0	1	1	0	1	0.6500
1	0	0	1	1	1	0	0.6375
1	0	0	1	1	1	1	0.6250
1	0	1	0	0	0	0	0.6125
1	0	1	0	0	0	1	0.6000
1	0	1	0	0	1	0	0.5875
1	0	1	0	0	1	1	0.5750
1	0	1	0	1	0	0	0.5625
1	0	1	0	1	0	1	0.5500
1	0	1	0	1	1	0	0.5375
1	0	1	0	1	1	1	0.5250
1	0	1	1	0	0	0	0.5125
1	0	1	1	0	0	1	0.5000
1	1	1	1	1	1	1	OFF

APPLICATION INFORMATION

The design parameters for a typical VR11−compliant CPU core VR application are as follows:

- Maximum Input Voltage (V_{INMAX}) = 19 V
- Minimum Input Voltage (V_{INMIN}) = 8.0 V
- Output Voltage by VID Setting (V_{VID}) = 1.2375 V
- Maximum Output Current (I_O) = 14 A
- Droop Resistance (R_O) = 6.9 mΩ
- Nominal Output Voltage at 15 A Load (V_{OFL}) = 1.1409 V
- Static output voltage drop from no load to full load (ΔV) = V_{ONL} − V_{OFL} = 1.2375 V − 1.1409 V = 96.6 mV
- Maximum Output Current Step (ΔI_O) = 11 A
- Number of Phases (n) = 1
- Switching Frequency (f_{SW}) = 390 kHz
- Duty Cycle at Maximum Input Voltage (D_{MAX}) = 0.15 V
- Duty Cycle at Minimum Input Voltage (D_{MIN}) = 0.065

SETTING THE CLOCK FREQUENCY FOR PWM

The NCP5380/A operates in fixed frequency PWM mode during startup, for 100 μs after a VID change, and in current limit. In PWM operation, the NCP5380/A uses a fixed−frequency control architecture. The frequency is set by an external timing resistor (RT). The clock frequency determines the switching frequency, which relates directly to the switching losses and the sizes of the inductors and input and output capacitors. For example, a clock frequency of 300 kHz sets the switching frequency to 300 kHz. This selection represents the trade−off between the switching losses and the minimum sizes of the output filter components. To achieve a 300 kHz oscillator frequency at a VID voltage of 1.2 V, RT must be 391 kΩ. Alternatively, the value for RT can be calculated by using the following equation:

$$R_T = \frac{V_{VID} + 1.0\ V}{2 \times f_{sw} \times 9\ pF} - 16\ k\Omega \qquad \text{(eq. 1)}$$

Where:
9 pF and 16 kΩ are internal IC component values.
V_{VID} is the VID voltage in volts.
f_{SW} is the switching frequency in hertz.

For good initial accuracy and frequency stability, it is recommended to use a 1% resistor.

RAMP RESISTOR SELECTION

The ramp resistor (R_R) is used for setting the size of the internal PWM ramp. The value of this resistor is chosen to provide the best combination of thermal balance, stability, and transient response. Use this equation to determine a starting value:

$$R_R = \frac{A_R \times L}{3 \times A_D \times R_{DS} \times C_R} \qquad \text{(eq. 2)}$$

$$R_R = \frac{0.5 \times 360\ nH}{3 \times 5 \times 5.2\ m\Omega \times 5\ pF}$$

Where:
A_R is the internal ramp amplifier gain.
A_D is the current balancing amplifier gain.
R_{DS} is the total low−side MOSFET ON−resistance,
C_R is the internal ramp capacitor value.

Another consideration in the selection of RR is the size of the internal ramp voltage (see Equation 3). For stability and noise immunity, keep this ramp size larger than 0.5 V. Taking this into consideration, the value of RR is selected as 280 kΩ.

The internal ramp voltage magnitude can be calculated using:

$$V_R = \frac{A_R \times (1 - D) \times V_{VID}}{R_R \times C_R \times f_{sw}} \qquad \text{(eq. 3)}$$

$$V_R = \frac{0.5 \times (1 - 0.065) \times 1.2375\ V}{462\ k\Omega \times 5\ pF \times 280\ kHz} = 0.89\ V$$

The size of the internal ramp can be made larger or smaller. If it is made larger, then stability and transient response improves, but thermal balance degrades. Likewise, if the ramp is made smaller, then thermal balance improves at the sacrifice of transient response and stability. The factor of three in the denominator of Equation 2 sets a minimum ramp size that gives an optimal balance for good stability, transient response, and thermal balance.

COMP PIN RAMP

In addition to the internal ramp, there is a ramp signal on the COMP pin due to the droop voltage and output voltage ramps. This ramp amplitude adds to the internal ramp to produce the following overall ramp signal at the PWM input:

$$V_{RT} = \frac{V_R}{1 - \frac{2 \times (1 - D)}{f \times C_X \times R_O}} \qquad \text{(eq. 4)}$$

Where C_X is the total bulk capacitance, and R_O is the droop resistance of the regulator.

For this example, the overall ramp signal is 0.23 V.

SETTING THE SWITCHING FREQUENCY FOR RPM OPERATION

During the RPM operation, the NCP5380/A runs in pseudoconstant frequency if the load current is high enough for continuous current mode. While in DCM, the switching frequency is reduced with the load current in a linear manner. To save power with light loads, lower switching

frequency is usually preferred during RPM operation. However, the V_{CC} ripple specification of VR11 sets a limitation for the lowest switching frequency. Therefore, depending on the inductor and output capacitors, the switching frequency in RPM can be equal to, greater than, or less than its counterpart in PWM.

A resistor from RPM to GND sets the pseudo constant frequency as following:

$$R_{RPM} = \frac{2 \times R_T}{V_{VID} + 1.0\ V} \times \frac{A_R \times (1 - D) \times V_{VID}}{R_R \times C_R \times f_{sw}} - 0.5\ k\Omega \quad \text{(eq. 5)}$$

Where:
A_R is the internal ramp amplifier gain.
C_R is the internal ramp capacitor value.
R_R is an external resistor on the RAMPADJ pin to set the internal ramp magnitude.

Because R_R = 280 kΩ, the following resistance sets up 300 kHz switching frequency in RPM operation.

$$R_{RPM} = \frac{2 \times 280\ k\Omega}{1.2375\ V + 1.0\ V} \times \frac{0.5 \times (1 - 0.065) \times 1.2375\ V}{462\ k\Omega \times 5\ pF \times 300\ kHz} - 500\ \Omega = 208\ k\Omega$$

INDUCTOR SELECTION

The choice of inductance determines the ripple current of the inductor. Less inductance results in more ripple current, which increases the output ripple voltage and the conduction losses in the MOSFETs. However, this allows the use of smaller−size inductors, and for a specified peak−to−peak transient deviation, it allows less total output capacitance. Conversely, a higher inductance results in lower ripple current and reduced conduction losses, but it requires larger−size inductors and more output capacitance for the same peak−to−peak transient deviation. For a buck converter, the practical value for peak−to−peak inductor ripple current is less than 50% of the maximum dc current of that inductor. Equation 6 shows the relationship between the inductance, oscillator frequency, and peak−to−peak ripple current. Equation 7 can be used to determine the minimum inductance based on a given output ripple voltage.

$$I_R = \frac{V_{VID} \times (1 - D_{MIN})}{f_{sw} \times V_{RIPPLE}} \quad \text{(eq. 6)}$$

$$L \geq \frac{V_{VID} \times R_O \times (1 - D_{MIN})}{f_{sw} \times V_{RIPPLE}} \quad \text{(eq. 7)}$$

In this example, RO is assumed to be the ESR of the output capacitance, which results in an optimal transient response. Solving Equation 7 for a 16 mV peak−to−peak output ripple voltage yields:

$$L \geq \frac{1.2375\ V \times 6.9\ m\Omega \times (1 - 0.065)}{390\ kHz \times 16\ mV} = 1.3\ \mu H \quad \text{(eq. 8)}$$

If the resultant ripple voltage is less than the initially selected value, the inductor can be changed to a smaller value until the ripple value is met. This iteration allows optimal transient response and minimum output decoupling. In this example, the iteration showed that a 560 nH inductor was sufficient to achieve a good ripple.

The smallest possible inductor should be used to minimize the number of output capacitors. Choosing a 560 nH inductor is a good choice for a starting point, and it provides a calculated ripple current of 6.6 A. The inductor should not saturate at the peak current of 18.3 A, and it should be able to handle the sum of the power dissipation caused by the winding's average current (15 A) plus the ac core loss.

Another important factor in the inductor design is the DCR, which is used for measuring the inductor current. Too large of a DCR causes excessive power losses, whereas too small of a value leads to increased measurement error. For this example, an inductor with a DCR of 1.3 mΩ is used.

Selecting a Standard Inductor

After the inductance and DCR are known, select a standard inductor that best meets the overall design goals. It is also important to specify the inductance and DCR tolerance to maintain the accuracy of the system. Using 20% tolerance for the inductance and 15% for the DCR at room temperature are reasonable values that most manufacturers can meet.

Power Inductor Manufacturers

The following companies provide surface−mount power inductors optimized for high power applications upon request.

- Vishay Dale Electronics, Inc.
  (605) 665−9301
- Panasonic
  (714) 373−7334
- Sumida Electric Company
  (847) 545−6700
- NEC Tokin Corporation
  (510) 324−4110

Output Droop Resistance

The design requires that the regulator output voltage measured at the chipset pins decreases when the output current increases. The specified voltage drop corresponds to the droop resistance (R_O).

The output current is measured by low−pass filtering the voltage across the inductor or current sense resistor. The filter is implemented by the CS amplifier that is configured with R_{PH}, R_{CS}, and C_{CS}. The output resistance of the regulator is set by the following equations:

$$R_O = \frac{R_{CS}}{R_{PH}} \times R_{SENSE} \quad \text{(eq. 9)}$$

$$C_{CS} = \frac{L}{R_{SENSE} \times R_{CS}} \quad \text{(eq. 10)}$$

Where R_{SENSE} is the DCR of the output inductors.

Either RCS or RPH can be chosen for added flexibility. Due to the current drive ability of the CSCOMP pin, the RCS resistance should be greater than 100 kΩ. For example, initially select RCS to be equal to 200 kΩ, and then use Equation 10 to solve for CCS:

$$C_{CS} = \frac{560\ nH}{1.3\ m\Omega \times 200\ k\Omega} = 2.2\ nF$$

If C_{CS} is not a standard capacitance, R_{CS} can be tuned. In this case, the required C_{CS} is a standard value and no tuning is required. For best accuracy, C_{CS} should be a 5% NPO capacitor.

Next, solve for RPH by rearranging Equation 9 as follows:

$$R_{PH} \geq \frac{1.3\ m\Omega}{5.1\ m\Omega} \times 200\ k\Omega = 51.0\ k\Omega$$

The standard 1% resistor for R_{PH} is 51.1 kΩ.

Inductor DCR Temperature Correction

If the DCR of the inductor is used as a sense element and copper wire is the source of the DCR, the temperature changes associated with the inductor's winding must be compensated for. Fortunately, copper has a well−known temperature coefficient (TC) of 0.39%/°C.

If RCS is designed to have an opposite but equal percentage of change in resistance, it cancels the temperature variation of the inductor's DCR. Due to the nonlinear nature of NTC thermistors, series resistors RCS1 and RCS2 (see Figure 24) are needed to linearize the NTC and produce the desired temperature coefficient tracking.

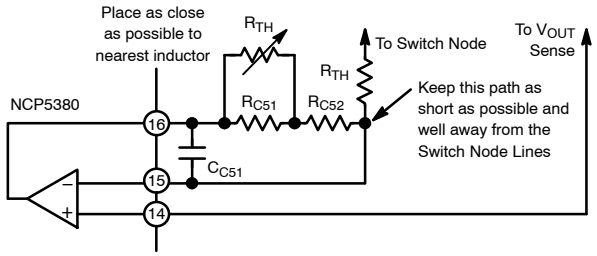


Figure 24. Temperature−Compensation Circuit Values

The following procedure and expressions yield values for R_{CS1}, R_{CS2}, and R_{TH} (the thermistor value at 25°C) for a given R_{CS} value.

1. Select an NTC to be used based on its type and value. Because the value needed is not yet determined, start with a thermistor with a value close to R_{CS} and an NTC with an initial tolerance of better than 5%.
2. Find the relative resistance value of the NTC at two temperatures. The appropriate temperatures will depend on the type of NTC, but 50°C and 90°C have been shown to work well for most types of NTCs. The resistance values are called A (A is $R_{TH}(50°C)/R_{TH}(25°C)$) and B (B is $R_{TH}(90°C)/R_{TH}(25°C)$). Note that the relative value of the NTC is always 1 at 25°C.
3. Find the relative value of R_{CS} required for each of the two temperatures. The relative value of R_{CS} is based on the percentage of change needed, which is initially assumed to be 0.39%/°C in this example. The relative values are called r_1 (r_1 is $1/(1+ TC \times (T_1 - 25))$) and r_2 (r_2 is $1/(1 + TC \times (T_2 - 25))$), where TC is 0.0039, T_1 is 50°C, and T_2 is 90°C.
4. Compute the relative values for r_{CS1}, r_{CS2}, and r_{TH} by using the following equations:

$$r_{cs} = \frac{(A - B) \times r_1 \times r_2 - A \times (1 - B) \times r_2 + B \times (1 - A) \times r_1}{A \times (1 - B) \times r_1 - B \times (1 - A) \times r_2 - (A - B)}$$

$$r_{CS1} = \frac{(1 - A)}{\frac{1}{1 - r_{CS2}} - \frac{A}{r_1 - r_{CS2}}}$$

$$r_{TH} = \frac{(1)}{\frac{1}{1 - r_{CS2}} - \frac{1}{r_{CS2}}}$$

5. Calculate $R_{TH} = r_{TH} \times R_{CS}$, and then select a thermistor of the closest value available. In addition, compute a scaling factor k based on the ratio of the actual thermistor value used relative to the computed one:

$$k = \frac{R_{TH(ACTUAL)}}{R_{TH(CALCULATED)}} \qquad \text{(eq. 11)}$$

6. Calculate values for R_{CS1} and R_{CS2} by using the following equations:

$$R_{CS1} = R_{CS} \times k \times r_{CS1} \qquad \text{(eq. 12)}$$

$$R_{CS2} = R_{CS} \times \left((1 - k) + \left(k \times r_{CS2}\right)\right)$$

For example, if a thermistor value of 100 kΩ is selected in Step 1, an available 0603−size thermistor with a value close to R_{CS} is the Vishay NTHS0603N04 NTC thermistor, which has resistance values of A = 0.3359 and B = 0.0771. Using the equations in Step 4, r_{CS1} is 0.359, r_{CS2} is 0.729, and r_{TH} is 1.094. Solving for r_{TH} yields 219 kΩ, so a thermistor of 220 kΩ would be a reasonable selection, making k equal to 1.005. Finally, R_{CS1} and R_{CS2} are found to be 72.2 kΩ and 146 kΩ. Choosing the closest 1% resistor values yields a choice of 71.5 kΩ and 147 kΩ.

C_{out} SELECTION

The required output decoupling for processors and platforms is typically recommended by Intel. For systems containing both bulk and ceramic capacitors, however, the following guidelines can be a helpful supplement.

Select the number of ceramics and determine the total ceramic capacitance (C_Z). This is based on the number and type of capacitors used. Keep in mind that the best location to place ceramic capacitors is inside the socket; however, the

physical limit is twenty 0805−size pieces inside the socket. Additional ceramic capacitors can be placed along the outer edge of the socket. A combined ceramic capacitor value of 40 μF to 50 μF is recommended and is usually composed of multiple 10 μF or 22 μF capacitors.

Ensure that the total amount of bulk capacitance (C_X) is within its limits. The upper limit is dependent on the VID OTF output voltage stepping (voltage step, V_V, in time, t_V, with error of V_{ERR}); the lower limit is based on meeting the critical capacitance for load release at a given maximum load step, ΔI_O. The current version of the VR11 specification allows a maximum V_{CC} overshoot (V_{OSMAX}) of 10 mV more than the VID voltage for a step−off load current.

$$C_{x(MIN)} \geq \left(\frac{L \times \Delta I_O}{\left(R_O + \frac{V_{OSMAX}}{\Delta I_O} \times V_{VID} \right)} - C_z \right) \quad \text{(eq. 13)}$$

$$C_{x(MAX)} \leq \frac{L}{k^2 \times R_O{}^2} \times \frac{V_V}{V_{VID}} \left(\sqrt{1 + \left(t_v \frac{V_{VID}}{V_V} \times \frac{k \times R_O}{L} \right)^2} - 1 \right) - C_Z \quad \text{(eq. 14)}$$

$$\text{Where } k = -\ln\left(\frac{V_{ERR}}{V_V} \right)$$

To meet the conditions of these expressions and the transient response, the ESR of the bulk capacitor bank (R_X) should be less than two times the droop resistance, R_O. If the $C_{X(MIN)}$ is greater than $C_{X(MAX)}$, the system does not meet the VID OTF specifications and may require less inductance. In addition, the switching frequency may have to be increased to maintain the output ripple.

For example, if two pieces of 22 μF, 0805−size MLC capacitors (C_Z = 44 μF) are used during a VID voltage change, the V_{CC} change is 220 mV in 22 μs with a setting error of 10 mV. If k = 3.1, solving for the bulk capacitance yields:

$$C_{X(MIN)} \geq \left(\frac{560\ nH \times 8\ A}{(5.1\ m\Omega) + \frac{10\ mV}{8\ A} \times 1.174\ V} - 44\ \mu F \right)$$

$$= 246\ \mu F$$

$$C_{X(MAX)} \leq \frac{560\ nH \times 220\ mV}{3.1^2 \times (5.1\ m\Omega)^2 \times 1.174\ V} \times \left(\sqrt{1 + \left(\frac{22\ \mu s \times 1.174\ V \times 3.1 \times 5.1\ m\Omega}{220\ mV \times 560\ nH} - 1 \right)} - 44\ \mu F \right)$$

$$= 992\ \mu F$$

Using two 220 μF Panasonic SP capacitors with a typical ESR of 7 mΩ each yields C_X = 440 μF and R_X = 3.5 mΩ.

Ensure that the ESL of the bulk capacitors (L_X) is low enough to limit the high frequency ringing during a load change. This is tested using:

$$L_X \leq C_Z \times R_O{}^2 \times Q^2 \quad \text{(eq. 15)}$$

$$L_X \leq 44\ \mu F \times (5.1\ m\Omega)^2 \times 2 = 2.3\ nH$$

Where:
Q is limited to the square root of 2 to ensure a critically damped system.

L_X is about 450 pH for the two SP capacitors, which is low enough to avoid ringing during a load change. If the L_X of the chosen bulk capacitor bank is too large, the number of ceramic capacitors may need to be increased to prevent excessive ringing.

For this multimode control technique, an all ceramic capacitor design can be used if the conditions of Equations 13, 14, and 15 are satisfied.

POWER MOSFETS

For typical 15 A applications, the N−channel power MOSFETs are selected for one high−side switch and two low−side switch. The main selection parameters for the power MOSFETs are $V_{GS(TH)}$, Q_G, C_{ISS}, C_{RSS}, and $R_{DS(ON)}$. Because the voltage of the gate driver is 5.0 V, logic−level threshold MOSFETs must be used.

The maximum output current, I_O, determines the $R_{DS(ON)}$ requirement for the low−side (synchronous) MOSFETs. With conduction losses being dominant, the following expression shows the total power that is dissipated in each synchronous MOSFET in terms of the ripple current per phase (I_R) and the average total output current (I_O):

$$P_{SF} = (1 - D) \times \left[\left(\frac{I_O}{\eta_{SF}} \right)^2 + \frac{1}{12} \times \left(\frac{I_R}{\eta_{SF}} \right)^2 \right] \times R_{DS(SF)} \quad \text{(eq. 16)}$$

where:
D is the duty cycle and is approximately the output voltage divided by the input voltage.
I_R is the inductor peak−to−peak ripple current and is approximately:

$$I_R = \frac{(1 - D) \times V_{OUT}}{L \times f_{sw}}$$

Knowing the maximum output current and the maximum allowed power dissipation, the user can calculate the required $R_{DS(ON)}$ for the MOSFET. For an 8−lead SOIC or 8−lead SOIC−compatible MOSFET, the junction−to−ambient (PCB) thermal impedance is 50°C/W. In the worst case, the PCB temperature is 70°C to 80°C during heavy load operation of the notebook, and a safe limit for P_{SF} is about 0.8 W to 1.0 W at 120°C junction temperature. Therefore, for this example (15 A maximum), the $R_{DS(SF)}$ per MOSFET is less than 18.8 mΩ for the

low−side MOSFET. This $R_{DS(SF)}$ is also at a junction temperature of about 120°C; therefore, the $R_{DS(SF)}$ per MOSFET should be less than 13.3 mΩ at room temperature, or 18.8 mΩ at high temperature.

Another important factor for the synchronous MOSFET is the input capacitance and feedback capacitance. The ratio of the feedback to input must be small (less than 10% is recommended) to prevent accidentally turning on the synchronous MOSFETs when the switch node goes high.

The high−side (main) MOSFET must be able to handle two main power dissipation components: conduction losses and switching losses. Switching loss is related to the time for the main MOSFET to turn on and off and to the current and voltage that are being switched. Basing the switching speed on the rise and fall times of the gate driver impedance and MOSFET input capacitance, the following expression provides an approximate value for the switching loss per main MOSFET:

$$P_{S(MF)} = 2 \times f_{SW} \times \frac{V_{DS} \times I_O}{\eta_{MF}} \times R_G \times \eta_{MF} \times C_{ISS} \quad \text{(eq. 17)}$$

Where:
n_{MF} is the total number of main MOSFETs.
R_G is the total gate resistance.
C_{ISS} is the input capacitance of the main MOSFET.

The most effective way to reduce switching loss is to use lower gate capacitance devices.

The conduction loss of the main MOSFET is given by the following equation:

$$P_{C(MF)} = D \times \left[\left(\frac{I_O}{\eta_{MF}} \right)^2 + \frac{1}{12} \times \left(\frac{I_R}{\eta_{MF}} \right)^2 \right] \times R_{DS(MF)} \quad \text{(eq. 18)}$$

Where $R_{DS(MF)}$ is the on resistance of the MOSFET.

Typically, a user wants the highest speed (low C_{ISS}) device for a main MOSFET, but such a device usually has higher on resistance. Therefore, the user must select a device that meets the total power dissipation (about 0.8 W to 1.0 W for an 8−lead SOIC) when combining the switching and conduction losses.

For example, an NTMFS4821N device can be selected as the main MOSFET (one in total; that is, n_{MF} = 1), with approximately C_{ISS} = 1400 pF (maximum) and $R_{DS(MF)}$ = 8.6 mΩ (maximum at T_J = 120°C), and an NTMFS4846N device can be selected as the synchronous MOSFET (two in total; that is, n_{SF} = 2), with $R_{DS(SF)}$ = 3.8 mΩ (maximum at T_J = 120°C). Solving for the power dissipation per MOSFET at I_O = 15 A and I_R = 5.0 A yields 178 mW for each synchronous MOSFET and 446 mW for each main MOSFET. A third synchronous MOSFET is an option to further increase the conversion efficiency and reduce thermal stress.

Finally, consider the power dissipation in the driver. This is best described in terms of the Q_G for the MOSFETs and is given by the following equation:

$$P_{DRV} = \left[\frac{f_{sw}}{2 \times n} \times \left(n_{MF} \times Q_{QFM} + n_{SF} \times Q_{GSF} \right) + I_{CC} \right] \times V_{CC} \quad \text{(eq. 19)}$$

where Q_{GMF} is the total gate charge for each main MOSFET, and Q_{GSF} is the total gate charge for each synchronous MOSFET.

The previous equation also shows the standby dissipation (I_{CC} times the V_{CC}) of the driver.

Current Limit Setpoint

To select the current−limit set point, we need to find the resistor value for R_{LIM}. The current−limit threshold for the NCP5380/A is set when the current in R_{LIM} is equal to the internal reference current of 20 μA. The current in R_{LIM} is equal to the inductor current times R_o. R_{LIM} can be found using the following equation:

$$R_{LIM} = \frac{I_{LIM} \times R_O}{20\ \mu A} \quad \text{(eq. 20)}$$

Where:
R_{LIM} is the current limit resistor. R_{LIM} is connected from the I_{LIM} pin to the CSCOMP pin.
R_O is the output load line resistance.
I_{LIM} is the current limit set point. This is the peak inductor current that will trip current limit.

In this example, if choosing 20 A for I_{LIM}, R_{LIM} is 6.9 kΩ, which is close to a standard 1% resistance of 6.98 kΩ.

The per−phase current limit described earlier has its limit determined by the following:

$$I_{PHLIM} \cong \frac{V_{COMP(MAX)} - V_R - V_{BIAS}}{A_D \times R_{DS(MAX)}} + \frac{I_R}{2} \quad \text{(eq. 21)}$$

For the NCP5380/A, the maximum COMP voltage ($V_{COMP(MAX)}$) is 3.3 V, the COMP pin bias voltage (V_{BIAS}) is 1.0 V, and the current balancing amplifier gain (A_D) is 5. Using a V_R of 0.55 V, and a $R_{DS(MAX)}$ of 3.8 mΩ (low−side on−resistance at 150°C) results in a per−phase limit of 85 A. Although this number seems high, this current level can only be reached with a absolute short at the output and the current−limit latchoff function shutting down the regulator before overheating occurs.

This limit can be adjusted by changing the ramp voltage V_R. However, users should not set the per−phase limit lower than the average per−phase current (I_{LIM}/n).

There is also a per−phase initial duty−cycle limit at maximum input voltage:

$$D_{LIM} = D_{MIN} \times \frac{V_{COMP(MAX)} - V_{BIAS}}{V_R} \quad \text{(eq. 22)}$$

Current Monitor

The NCP5380/A has an output current monitor. The IMON pin sources a current proportional to the total inductor current. A resistor, R_{MON}, from IMON to FBRTN

sets the gain of the output current monitor. A 0.1 μF is placed in parallel with R_{MON} to filter the inductor current ripple and high frequency load transients. Since the IMON pin is connected directly to the CPU, it is clamped to prevent it from going above 1.15 V.

The IMON pin current is equal to the R_{LIM}times a fixed gain of 10. R_{MON} can be found using the following equation:

$$R_{MON} = \frac{1.15\ V \times R_{LIM}}{10 \times R_O \times I_{FS}} \quad \text{(eq. 23)}$$

Where:
R_{MON} is the current monitor resistor. R_{MON} is connected from IMON pin to FBRTN.
R_{LIM} is the current limit resistor.
R_O is the output load line resistance.
I_{FS} is the output current when the voltage on IMON is at full scale.

Feedback Loop Compensation Design

Optimized compensation of the NCP5380/A allows the best possible response of the regulator's output to a load change. The basis for determining the optimum compensation is to make the regulator and output decoupling appear as an output impedance that is entirely resistive over the widest possible frequency range, including dc, and that is equal to the droop resistance (R_O). With the resistive output impedance, the output voltage droops in proportion with the load current at any load current slew rate, ensuring the optimal position and allowing the minimization of the output decoupling.

With the multimode feedback structure of the NCP5380/A, it is necessary to set the feedback compensation so that the converter's output impedance works in parallel with the output decoupling. In addition, it is necessary to compensate for the several poles and zeros created by the output inductor and decoupling capacitors (output filter).

A Type III compensator on the voltage feedback is adequate for proper compensation of the output filter. Figure 25 shows the Type III amplifier used in the NCP5380/A. Figure 26 shows the locations of the two poles and two zeros created by this amplifier.

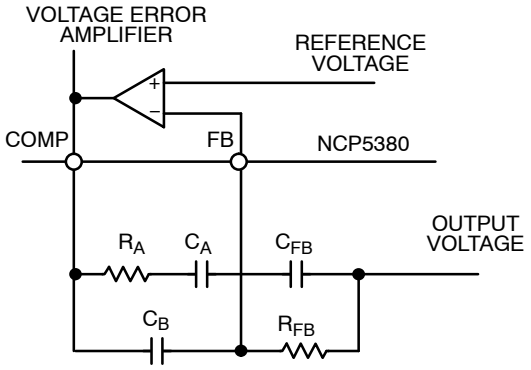


Figure 25. Voltage Error Amplifier

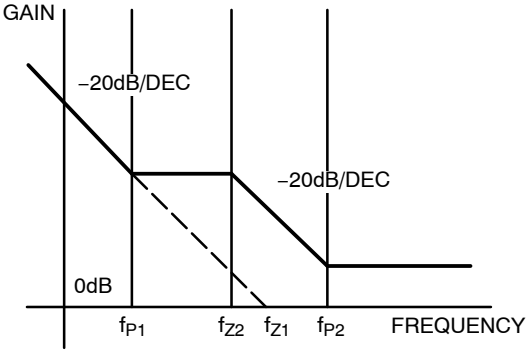


Figure 26. Poles and Zeros of Voltage Error

The following equations give the locations of the poles and zeros shown in Figure 26:

$$f_{Z1} = \frac{1}{2\pi \times C_A \times R_A} \quad \text{(eq. 24)}$$

$$f_{Z2} = \frac{1}{2\pi \times C_{FB} \times R_{FB}} \quad \text{(eq. 25)}$$

$$f_{P1} = \frac{1}{2\pi\left(C_A + C_B\right) \times R_{FB}} \quad \text{(eq. 26)}$$

$$f_{P2} = \frac{1}{2\pi \times R_A \times C_B \times C_A} \quad \text{(eq. 27)}$$

The expressions that follow compute the time constants for the poles and zeros in the system and are intended to yield an optimal starting point for the design; some adjustments may be necessary to account for PCB and component parasitic effects (see the Tuning Procedure for NCP5380/A section):

$$R_E = R_O + A_D \times R_{DS} + \frac{R_L \times V_{RT}}{V_{VID}} + \frac{2 \times L \times (1 - (n \times D)) \times V_{RT}}{C_X \times R_O \times V_{VID}} \quad \text{(eq. 28)}$$

$$T_A = C_X \times \left(R_O - R'\right) + \frac{L_X}{R_O} \times \frac{R_O - R'}{R_X} \quad \text{(eq. 29)}$$

$$T_B = \left(R_X + R' - R_O\right) \times C_X \quad \text{(eq. 30)}$$

$$T_C = \frac{V_{RT} \times \left(L - \frac{A_D \times R_{DS}}{2 \times f}\right)}{V_{VID} \times R_E} \quad \text{(eq. 31)}$$

$$T_D = \frac{C_X \times C_Z \times R_O{}^2}{C_X \times \left(R_O - R'\right) + C_Z \times R_O} \quad \text{(eq. 32)}$$

Where:
R' is the PCB resistance from the bulk capacitors to the ceramics and is approximately 0.4 mΩ (assuming an 8−layer motherboard).
R_{DS} is the total low−side MOSFET for on resistance.
A_D is 5.
V_{RT} is 1.25 V.
L_X is the ESL of the bulk capacitors (450 pH for the two Panasonic SP capacitors).

The compensation values can be calculated as follows:

$$C_A = \frac{R_O \times T_A}{R_E \times R_B} \quad \text{(eq. 33)}$$

$$R_A = \frac{T_C}{C_A} \quad \text{(eq. 34)}$$

$$C_B = \frac{T_B}{R_B} \quad \text{(eq. 35)}$$

$$C_{FB} = \frac{T_D}{R_A} \quad \text{(eq. 36)}$$

The standard values for these components are subject to the tuning procedure described in the Tuning Procedure for NCP5380/A section.

C_{IN} Selection and Input Current di/dt Reduction

In continuous inductor−current mode, the source current of the high−side MOSFET is approximately a square wave with a duty ratio equal to V_{OUT}/V_{IN}. To prevent large voltage transients, use a low ESR input capacitor sized for the maximum rms current. The maximum rms capacitor current occurs at the lowest input voltage and is given by

$$I_{CRMS} = D \times 1_O \times \sqrt{\frac{1}{D} - 1} \quad \text{(eq. 37)}$$

$$I_{CRMS} = 0.15 \times 15\ A \times \frac{\sqrt{\frac{1}{0.15} - 1}}{5.36}\ A$$

Where I_O is the output current.

In a typical notebook system, the battery rail decoupling is achieved by using MLC capacitors or a mixture of MLC capacitors and bulk capacitors. In this example, the input capacitor bank is formed by four pieces of 10 μF, 25 V MLC capacitors, with a ripple current rating of about 1.5 A each.

SOFT TRANSIENT SETTING

As described in the Theory of Operation section, during the soft transient, the slew rate of the V_{CC} reference voltage change is controlled by the ST pin capacitance. The ST pin capacitance is set to satisfy the slew rate for a fast exit as follows:

$$C_{ST} = \frac{7.5\ \mu A}{SLEWRATE} \quad \text{(eq. 38)}$$

Where:
7.5 μA is the source/sink current of the ST pin.
SLEWRATE is the voltage slew rate after a change in VID voltage
and is defined as 10 mV/μA in the VR11 specification.
CST is 750 pF, and the closest standard capacitance is 680 pF.

TUNING PROCEDURE FOR NCP5380

Set−Up and Test the Circuit

1. Build a circuit based on the compensation values computed from the design spreadsheet.
2. Connect a dc load to the circuit.
3. Turn on the NCP5380/A and verify that it operates properly.
4. Check for jitter with no load and full load conditions.

Set the DC Load Line

1. Measure the output voltage with no load (V_{NL}) and verify that this voltage is within the specified tolerance range.
2. Measure the output voltage with a full load when the device is cold (VFLCOLD). Allow the board to run for ~10 minutes with a full load and then measure the output when the device is hot (VFLHOT). If the difference between the two measured voltages is more than a few millivolts, adjust RCS2 using Equation 39.

$$R_{CS2(NEW)} = R_{CS2(OLD)} \times \frac{V_{NL} - V_{FLCOLD}}{V_{NL} - V_{FLHOT}} \quad \text{(eq. 39)}$$

3. Repeat Step 2 until no adjustment of R_{CS2} is needed.
4. Compare the output voltage with no load to that with a full load using 5 A steps. Compute the load line slope for each change and then find the average to determine the overall load line slope (R_{OMEAS}).
5. If the difference between R_{OMEAS} and R_O is more than 0.05 mΩ, use the following equation to adjust the R_{PH} values:

$$R_{PH(NEW)} = R_{PH(OLD)} \times \frac{R_{OMEAS}}{R_O} \quad \text{(eq. 40)}$$

6. Repeat Steps 4 and 5 until no adjustment of R_{PH} is needed. Once this is achieved, do not change R_{PH}, R_{CS1}, R_{CS2}, or R_{TH} for the rest of the procedure.
7. Measure the output ripple with no load and with a full load with scope, making sure both are within the specifications.

Set the AC Load Line

1. Remove the dc load from the circuit and connect a dynamic load.
2. Connect the scope to the output voltage and set it to dc coupling mode with a time scale of 100 μs/div.
3. Set the dynamic load for a transient step of about 40 A at 1 kHz with 50% duty cycle.
4. Measure the output waveform (note that use of a dc offset on the scope may be necessary to see the waveform). Try to use a vertical scale of 100 mV/div or finer.
5. Do not measure the undershoot or overshoot that occurs immediately after the step.

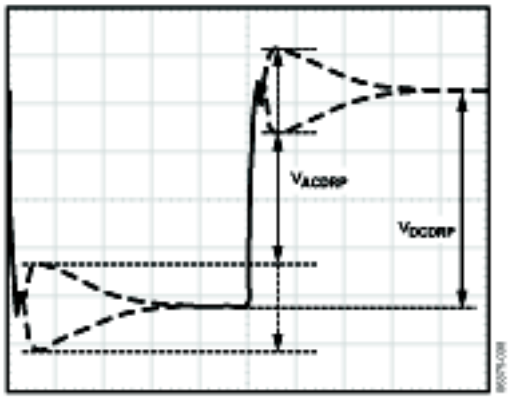


Figure 27. AC Load Line Waveform

6. If the difference between V_{ACDRP} and V_{DCDRP} is more than a couple of millivolts, use Equation 42 to adjust C_{CS}. It may be necessary to try several parallel values to obtain an adequate one because there are limited standard capacitor values available (it is a good idea to have locations for two capacitors in the layout for this reason).

$$C_{CS(NEW)} = C_{CS(OLD)} \times \frac{V_{ACDRP}}{V_{DCDRP}} \qquad \text{(eq. 41)}$$

7. Repeat Steps 5 and 6 until no adjustment of C_{CS} is needed. Once this is achieved, do not change C_{CS} for the rest of the procedure.
8. Set the dynamic load step to its maximum step size (but do not use a step size that is larger than needed) and verify that the output waveform is square, meaning V_{ACDRP} and V_{DCDRP} are equal.
9. Ensure that the load step slew rate and the power−up slew rate are set to ~150 A/μs to 250 A/μs (for example, a load step of 50 A should take 200 ns to 300 ns) with no overshoot. Some dynamic loads have an excessive overshoot at power−up if a minimum current is incorrectly set (this is an issue if a VTT tool is in use).

Set the Initial Transient

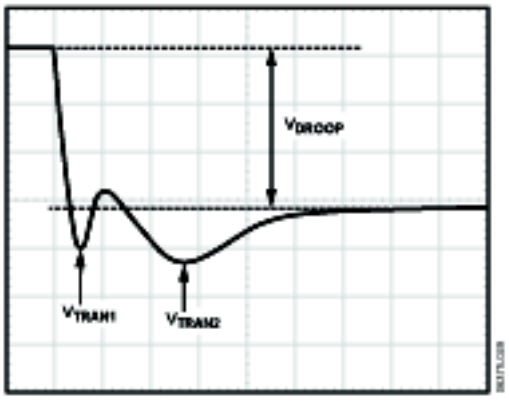


Figure 28. Transient Setting Waveform, Load Step

1. With the dynamic load set at its maximum step size, expand the scope time scale to 2 μs/div to 5 μs/div. This results in a waveform that may have two overshoots and one minor undershoot before achieving the final desired value after VDROOP (see Figure 28).
2. If both overshoots are larger than desired, try the following adjustments in the order shown.
   a. Increase the resistance of the ramp resistor (R_{RAMP}) by 25%.
   b. For V_{TRAN1}, increase C_B or increase the switching frequency.
   c. For V_{TRAN2}, increase R_A by 25% and decrease C_A by 25%.

   If these adjustments do not change the response, it is because the system is limited by the output decoupling. Check the output response and the switching nodes each time a change is made to ensure that the output decoupling is stable.
3. For load release (see Figure 29), if $V_{TRANREL}$ is larger than the value specified by VR11, a greater percentage of output capacitance is needed. Either increase the capacitance directly or decrease the inductor values. (If inductors are changed, however, it will be necessary to redesign the circuit using the information from the spreadsheet and to repeat all tuning guide procedures).

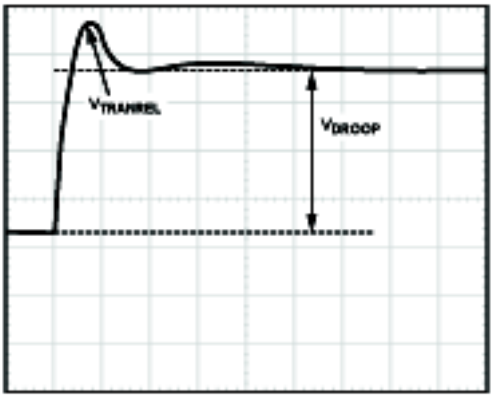


Figure 29. Transient Setting Waveform, Load Release

LAYOUT AND COMPONENT PLACEMENT

The following guidelines are recommended for optimal performance of a switching regulator in a PC system.

General Recommendations

1. For best results, use a PCB of four or more layers. This should provide the needed versatility for control circuitry interconnections with optimal placement; power planes for ground, input, and output; and wide interconnection traces in the rest of the power delivery current paths. Keep in mind that each square unit of 1 oz copper trace has a resistance of ~0.53 mΩ at room temperature.
2. When high currents must be routed between PCB layers, vias should be used liberally to create several parallel current paths so that the resistance and inductance introduced by these current paths is minimized and the via current rating is not exceeded.
3. If critical signal lines (including the output voltage sense lines of the NCP5380/A) must cross through power circuitry, it is best if a signal ground plane can be interposed between those signal lines and the traces of the power circuitry. This serves as a shield to minimize noise injection into the signals at the expense of increasing signal ground noise.
4. An analog ground plane should be used around and under the NCP5380/A for referencing the components associated with the controller. This plane should be tied to the nearest ground of the output decoupling capacitor, but should not be tied to any other power circuitry to prevent power currents from flowing into the plane.
5. The components around the NCP5380/A should be located close to the controller with short traces. The most important traces to keep short and away from other traces are those to the FB and CSFB pins. Refer to Figure 24 for more details on the layout for the CSFB node.
6. The output capacitors should be connected as close as possible to the load (or connector) that receives the power (for example, a microprocessor core). If the load is distributed, the capacitors should also be distributed and generally placed in greater proportion where the load is more dynamic.
7. Avoid crossing signal lines over the switching power path loop, as described in the Power Circuitry section.

Power Circuitry

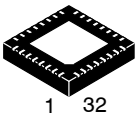
1. The switching power path on the PCB should be routed to encompass the shortest possible length to minimize radiated switching noise energy (that is, EMI) and conduction losses in the board. Failure to take proper precautions often results in EMI problems for the entire PC system as well as noise−related operational problems in the power−converter control circuitry. The switching power path is the loop formed by the current path through the input capacitors and the power MOSFETs, including all interconnecting PCB traces and planes. The use of short, wide interconnection traces is especially critical in this path for two reasons: it minimizes the inductance in the switching loop, which can cause high energy ringing, and it accommodates the high current demand with minimal voltage loss.
2. When a power−dissipating component (for example, a power MOSFET) is soldered to a PCB, the liberal use of vias, both directly on the mounting pad and immediately surrounding it, is recommended. Two important reasons for this are improved current rating through the vias and improved thermal performance from vias extended to the opposite side of the PCB, where a plane can more readily transfer heat to the surrounding air. To achieve optimal thermal dissipation, mirror the pad configurations used to heat sink the MOSFETs on the opposite side of the PCB. In addition, improvements in thermal performance can be obtained using the largest possible pad area.
3. The output power path should also be routed to encompass a short distance. The output power path is formed by the current path through the inductor, the output capacitors, and the load.
4. For best EMI containment, a solid power ground plane should be used as one of the inner layers and extended under all power components.

Signal Circuitry

1. The output voltage is sensed and regulated between the FB and FBRTN pins, and the traces of these pins should be connected to the signal ground of the load. To avoid differential mode noise pickup in the sensed signal, the loop area should be as small as possible. Therefore, the FB and FBRTN traces should be routed adjacent to each other, atop the power ground plane, and back to the controller.
2. The feedback traces from the switch nodes should be connected as close as possible to the inductor. The CSREF signal should be Kelvin connected to the center point of the copper bar, which is the V_{CC} common node for the inductor.
3. On the back of the NCP5380/A package, there is a metal pad that can be used to heat sink the device. Therefore, running vias under the NCP5380/A is not recommended because the metal pad may cause shorting between vias.

QFN32 5x5, 0.5P
CASE 488AM
ISSUE A

DATE 23 OCT 2013



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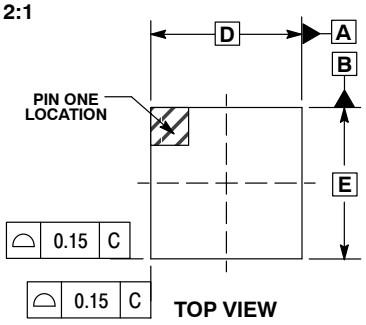
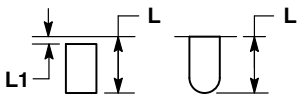
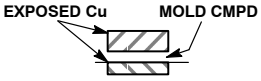


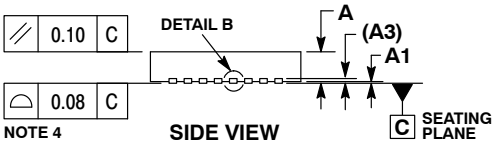
TOP VIEW



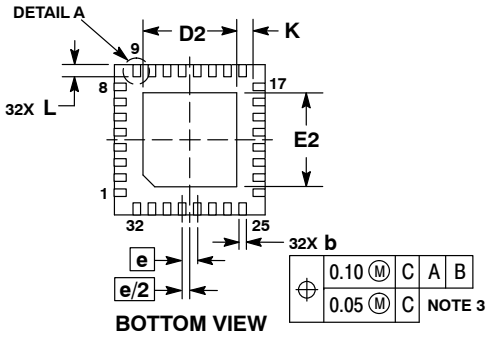
DETAIL A
ALTERNATE TERMINAL CONSTRUCTIONS



DETAIL B
ALTERNATE CONSTRUCTION



SIDE VIEW

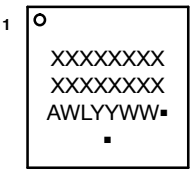


BOTTOM VIEW

NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	---	0.05
A3	0.20 REF	
b	0.18	0.30
D	5.00 BSC	
D2	2.95	3.25
E	5.00 BSC	
E2	2.95	3.25
e	0.50 BSC	
K	0.20	---
L	0.30	0.50
L1	---	0.15

GENERIC MARKING DIAGRAM*

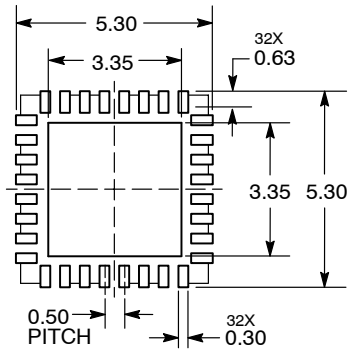


XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking.
Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSION: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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