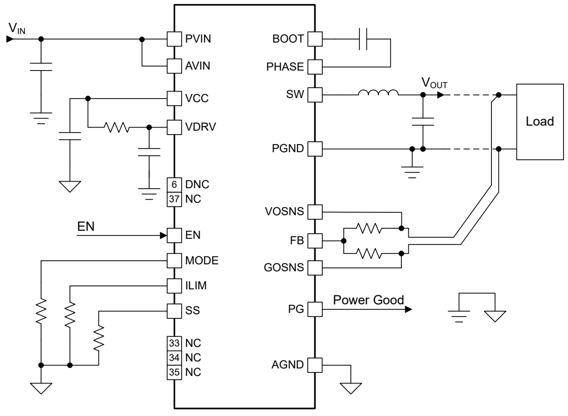
TPS548D26 4V to 16V Input, 40A Synchronous Buck Converter With Differential Remote Sense

1 Features

- Integrated 4.0mΩ and 1.0mΩ MOSFETs for 40A continuous current operation
- Supports external 5V bias improving efficiency and enabling 2.7V minimum input voltage
- 0.6V to 5.5V output voltage range
- Precision voltage reference and differential remote sense for high output accuracy
  - ±0.5% V_{OUT} tolerance from 0°C to 85°C T_J
  - ±1% V_{OUT} tolerance from –40°C to 125°C T_J
- D-CAP+™ control topology with fast transient response, supporting all ceramic output capacitors
- Selectable internal loop compensation through SS pin
- Selectable cycle-by-cycle valley current limit
- Selectable operation frequency 0.6MHz to 1.2MHz with DCM or FCCM operation
- Safe start-up into prebiased outputs
- Programmable soft-start time from 0.75ms to 6ms
- Open-drain power-good output (PG)
- Overcurrent, overvoltage, undervoltage, and overtemperature protections with selectable hiccup or latch-off response
- 5mm × 6mm, 37-pin WQFN-FCRLF package



Simplified Schematic

2 Applications

- Server and cloud-computing POLs
- Hardware accelerator
- Data center switches

3 Description

The TPS548D26 device is a highly integrated buck converter with D-CAP+ control topology for fast transient response. Because external compensation is not required, the device is easy to use and requires few external components. The device is well-designed for space-constrained data center applications.

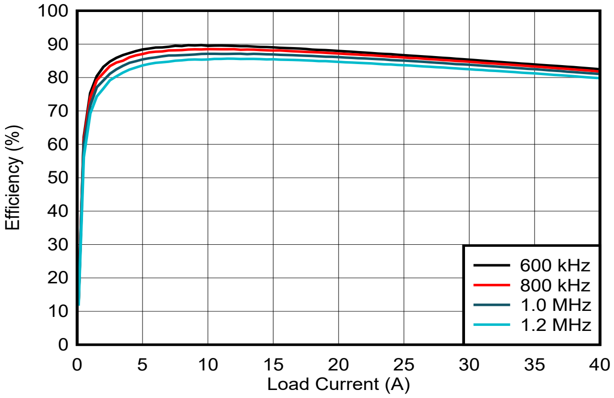
The TPS548D26 device has true differential remote sense, high-performance integrated MOSFETs, and an accurate ±1%, 0.6V reference over the full operating junction temperature range. The device features fast load-transient response, accurate load regulation and line regulation, skip-mode or FCCM operation, and programmable soft-start time. Overcurrent, overvoltage, undervoltage, and overtemperature protections are provided with selectable hiccup or latch-off response.

The TPS548D26 device is a lead-free device and is RoHS compliant without exemption.

Package Information

PART NUMBER	PACKAGE[1]	PACKAGE SIZE[2]
TPS548D26	RXX (WQFN-FCRLF, 37)	5.00mm × 6.00mm

(1) For more information, see Section 10.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



PVIN = 12V VCC = External 5V Bias V_{OUT} = 0.76V
MODE = FCCM

Typical Efficiency

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4 Pin Configuration and Functions

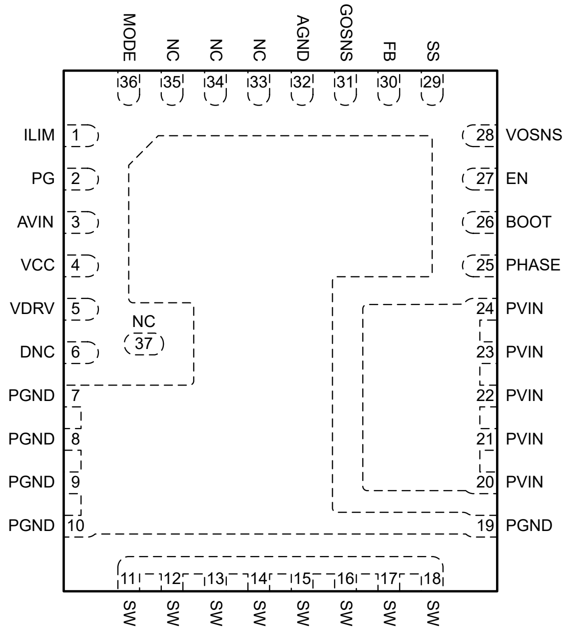


Figure 4-1. RXX 37-Pin WQFN-FCRLF Package (Top View)

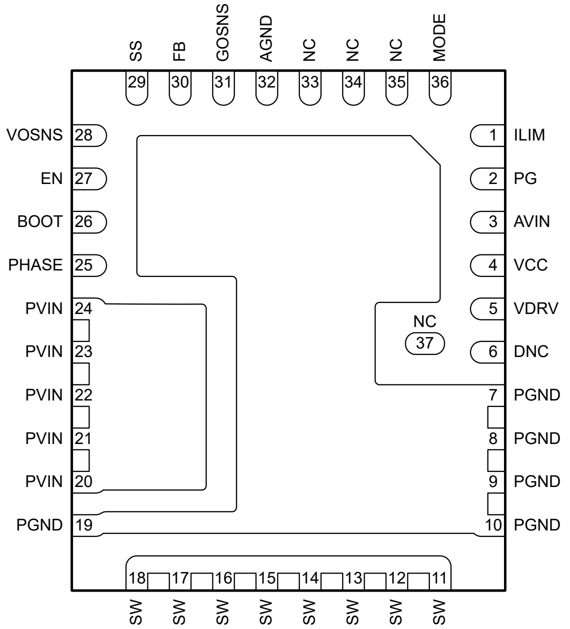


Figure 4-2. RXX 37-Pin WQFN-FCRLF Package (Bottom View)

Table 4-1. Pin Functions

PIN		TYPE[(1)]	DESCRIPTION
NAME	NO.		
AGND	32	G	Ground pin, reference point for internal control circuitry
AVIN	3	P	Supply rail for the internal VCC LDO. Connect a 1-µF, 25-V ceramic capacitor to AGND to bypass this pin.
BOOT	26	P	Supply rail for the high-side gate driver (boost terminal). Connect the bootstrap capacitor from this pin to PHASE pin. TI recommends a high temperature (X7R) 0.1 µF or greater value ceramic capacitor.
DNC	6	—	Do Not Connect (DNC) pin. This pin is the output of internal circuitry and must be floating. Pin 6 and pin 37 can be shorted together but NO any other PCB connection is allowed on pin 6.
EN	27	I	Enable pin, an active-high input pin that, when asserted high, causes the converter to begin the soft-start sequence for the output voltage rail. When de-asserted low, the converter de-asserts PG pin and begins the shutdown sequence of the output voltage rail and continue to completion.
FB	30	I	Positive input of the differential remote sense amplifier, connect to the center point of an external voltage divider. The voltage divider must be connected to output remote sense point.
GOSNS	31	I	Negative input of the differential remote sense circuit, connect to the ground sense point on the load side.
ILIM	1	I	Overcurrent limit selection pin. Connect a resistor to AGND to select the overcurrent limit threshold.
MODE	36	I	The MODE pin selects the switching frequency and sets the operation mode to FCCM or DCM, by connecting a resistor to AGND.
SS	29	I	The SS pin selects the soft-start time, internal compensation and the fault response, by connecting a resistor to AGND.
NC	33, 34, 35	—	No connection (NC) pin. There is no active circuit connected inside the IC. These pins can be connected to ground plane or left open.

Table 4-1. Pin Functions (continued)

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
NC	37	—	No connection (NC) pin. This pin is floating internally. Pin 37 and pin 6 can be shorted together.
PG	2	O	Power-good output signal. The PG indicator is asserted when the output voltage reaches the regulation. The PG indicator de-asserts low when the EN pin is pulled low or a shutdown fault occurs. This open-drain output requires an external pullup resistor.
PGND	7 – 10, 19	G	Power ground for the internal power stage.
PHASE	25	—	Return for high-side MOSFET driver. Shorted to SW internally. Connect the bootstrap capacitor from BOOT pin to this pin.
PVIN	20 – 24	P	Power input for both the power stage. PVIN is the input of the internal VCC LDO as well.
SW	11 – 18	O	Output switching terminal of the power converter. Connect these pins to the output inductor.
VCC	4	P	Internal VCC LDO output and also the input for the internal control circuitry. A 2.2-μF (or 1 μF), at least 6.3-V rating ceramic capacitor is required to be placed from VCC pin to AGND for decoupling.
VDRV	5	P	Power supply input for gate driver circuit. A 2.2-μF (or 4.7 μF), at least 6.3-V rating ceramic capacitor is required to be placed from VDRV pin to PGND pins to decouple the noise generated by driver circuitry. An external 5-V bias can be connected to this pin to save the power losses on the internal LDO.
VOSNS	28	I	Output voltage sense point for internal on-time generation circuitry. Ti recommends shorting this pin directly to the VOUT sense point. Adding any resistance higher than 51 Ω between VOUT sense point and the VOSNS pin shifts switching frequency higher than the desired setting. Contact Texas Instruments if a resistor has to be placed between the VOUT sense point and the VOSNS pin.

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power.

5 Specifications

5.1 Absolute Maximum Ratings

Over operating junction temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Pin voltage	PVIN	–0.3	18	V
Pin voltage	AVIN	–0.3	18	V
Pin voltage	PVIN – SW, DC	–0.3	18	V
Pin voltage	PVIN – SW, transient < 10 ns	–1.5	26	V
Pin voltage	SW – PGND, DC	–0.3	18	V
Pin voltage	SW – PGND, transient < 10 ns	–3.0	21.5	V
Pin voltage	BOOT – PGND	–0.3	23.5	V
Pin voltage	BOOT – SW	–0.3	5.5	V
Pin voltage	VCC, VDRV	–0.3	5.5	V
Pin voltage	PHASE	–0.3	18	V
Pin voltage	EN, VOSNS, ILIM, MODE, SS, FB, PG	–0.3	5.5	V
Pin voltage	GOSNS – AGND	–0.3	0.3	V
Pin voltage	DNC, NC	–0.3	1.9	V
Sink current	PG	0	10	mA
T_J	Operating junction temperature	–40	150	°C
T_{stg}	Storage temperature	–55	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002 (2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

Over operating junction temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{OUT}	Output voltage range		0.6		5.5	V
V_{IN}	Input voltage	PVIN when VCC and VDRV are powered by the internal LDO	4.0		16	V
		PVIN when VCC and VDRV are powered by an external 5-V bias	2.7		16	V
V_{IN}	Input voltage	AVIN	4.0		16	V
V_{BIAS}	Input voltage	VCC and VDRV external bias	4.75		5.3	V
I_{OUT}	Output current range				40	A
	Pin voltage	EN, PG	–0.1		5.3	V
I_{PG}	Power-good input current capability				10	mA
T_J	Operating junction temperature		–40		125	°C

5.4 Thermal Information

THERMAL METRIC(1)		DEVICE		UNIT
		RXX (QFN, JEDEC)	RXX (QFN, TI EVM)	
		37 PINS	37 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	25.4	15.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	3.6	Not applicable(2)	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	6.6	Not applicable(2)	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3.1	Not applicable(2)	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.1(3)	2.0(4)	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	3.6	5.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.
(2) The thermal test or simulation setup is not applicable to a TI EVM layout.
(3) The power dissipation is evenly distributed across all the silicon areas inside the package on the thermal simulation based on the JEDEC standard, resulting in the hot spot being centered in the package.
(4) The power dissipation is concentrated on the power FET area on the thermal simulation based on the TI EVM layout, resulting in the hot spot being offset inside the package.

5.5 Electrical Characteristics

T_J = –40°C to +125°C. PVIN = 4 V to 16 V, V_{VCC} = 4.5 V to 5.0 V (unless otherwise noted). Typical values are at T_J = 25°C, PVIN = 12 V and V_{VCC} = 4.5 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
	PVIN operating input range		4		16	V
	AVIN operating input range		4		16	V
$I_{Q(AVIN)}$	AVIN quiescent current	Non-switching, PVIN = 12 V, AVIN = 12 V, V_{EN} = 2 V, V_{FB} = V_{REF} + 50 mV, no bias on VCC and VDRV pin	5	6.3	7.5	mA
$I_{SD(PVIN)}$	PVIN shutdown supply current	PVIN = 12 V, AVIN = 12 V, V_{EN} = 0 V, no bias on VCC and VDRV pin		20		µA
I_{VCC}	VCC and VDRV external bias current	External 5-V bias on VCC and VDRV pin, regular switching. T_J = 25°C, PVIN = 12 V, I_{OUT} = 35 A, V_{EN} = 2 V, f_{SW} = 0.6 MHz		32.7		mA
I_{VCC}	VCC and VDRV external bias current	External 5-V bias on VCC and VDRV pin, regular switching. T_J = 25°C, PVIN = 12 V, I_{OUT} = 35 A, V_{EN} = 2 V, f_{SW} = 0.8 MHz		39.7		mA
I_{VCC}	VCC and VDRV external bias current	External 5-V bias on VCC and VDRV pin, regular switching. T_J = 25°C, PVIN = 12 V, I_{OUT} = 35 A, V_{EN} = 2 V, f_{SW} = 1.0 MHz		48.7		mA
I_{VCC}	VCC and VDRV external bias current	External 5-V bias on VCC and VDRV pin, regular switching. T_J = 25°C, PVIN = 12 V, I_{OUT} = 35 A, V_{EN} = 2 V, f_{SW} = 1.2 MHz		57.3		mA
$I_{SD(VCC\_VDRV)}$	VCC + VDRV shutdown supply current	External 5-V bias on VCC and VDRV pin, PVIN = 12 V, V_{EN} = 0 V	5	6.3	7.5	mA
UVLO						
$PVIN_{OV}$	PVIN overvoltage rising threshold	PVIN rising	18.0	18.6	19.2	V
$PVIN_{OV}$	PVIN overvoltage falling threshold	PVIN falling. PVIN_OVF status bit, after it is set, cannot be cleared unless PVIN falls below the PVIN overvoltage falling threshold	12.9	13.4	13.9	V
$PVIN_{UVLO(R)}$	PVIN UVLO rising threshold	PVIN rising, external 5-V bias on VCC and VDRV pin	2.35	2.55	2.75	V
$PVIN_{UVLO(F)}$	PVIN UVLO falling threshold	PVIN falling, external 5-V bias on VCC and VDRV pin	2.10	2.30	2.50	V
$PVIN_{UVLO(H)}$	PVIN UVLO hysteresis			0.25		V
ENABLE						
$V_{EN(R)}$	EN voltage rising threshold	EN rising, enable switching	1.14	1.19	1.24	V
$V_{EN(F)}$	EN voltage falling threshold	EN falling, disable switching	0.94	0.98	1.02	V

5.5 Electrical Characteristics (continued)

T_J = –40°C to +125°C. PVIN = 4 V to 16 V, V_{VCC} = 4.5 V to 5.0 V (unless otherwise noted). Typical values are at T_J = 25°C, PVIN = 12 V and V_{VCC} = 4.5 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{EN(H)}$	EN voltage hysteresis			0.21		V
$t_{EN(DIG)}$	EN Deglitch Time		0.2			µs
	EN internal pulldown resistor	V_{EN} = 2 V, EN pin to AGND	110	125	140	kΩ
INTERNAL VCC LDO						
	VCC LDO output voltage	AVIN= 4 V, $I_{VCC(load)}$ = 5 mA	3.925	3.97	4.0	V
	VCC LDO output voltage	AVIN= 5 V to 16 V, $I_{VCC(load)}$ = 5 mA	4.28	4.44	4.55	V
	VCC LDO dropout voltage	AVIN – V_{VCC}, AVIN = 4 V, $I_{VCC(load)}$ = 50 mA		160.8	280	mV
	VCC_OK rising threshold	T_J = –40°C to 85°C. VCC rising, enabling initial power-on including re-loading default values from NVM	3.0	3.15	3.3	V
	VCC_OK falling threshold	T_J = –40°C to 85°C. VCC falling, disabling controller circuit including the memory and the digital engine	2.95	3.10	3.25	V
	VCC LDO short-circuit current limit		150			mA
REFERENCE VOLTAGE						
V_{FB}	FB voltage	T_J = 0°C to 85°C	594	600	603	mV
V_{FB}	FB voltage	T_J = –40°C to 125°C	591	600	606	mV
$I_{FB(LKG)}$	FB input leakage current	V_{FB} = 600 mV		10		nA
SWITCHING FREQUENCY						
$f_{SW(FCCM)}$	Switching frequency, FCCM operation	T_J = –40°C to 125°C, PVIN = 12 V, V_{OUT} = 1.1 V, no load, R_{MODE} = 0 Ω	540	600	660	kHz
$f_{SW(FCCM)}$	Switching frequency, FCCM operation	T_J = –40°C to 125°C, PVIN = 12 V, V_{OUT} = 1.1 V, no load, R_{MODE} = 1.5 kΩ	720	800	880	kHz
$f_{SW(FCCM)}$	Switching frequency, FCCM operation	T_J = –40°C to 125°C, PVIN = 12 V, V_{OUT} = 1.1 V, no load, R_{MODE} = 14 kΩ	900	1000	1100	kHz
$f_{SW(FCCM)}$	Switching frequency, FCCM operation	T_J = –40°C to 125°C, PVIN = 12 V, V_{OUT} = 1.1 V, no load, R_{MODE} = 16.2 kΩ	1080	1200	1320	kHz
$f_{SW(FCCM)}$	Switching frequency, FCCM operation	T_J = –40°C to 125°C, PVIN = 12 V, V_{OUT} = 1.1 V, no load, R_{MODE} = float	720	800	880	kHz
STARTUP AND SHUTDOWN						
$t_{ON(DLY)}$	Power on sequence delay	V_{VCC} = 4.5 V		0.5	0.55	ms
$t_{ON(Rise)}$	Soft-start time	V_{VCC} = 4.5 V, R_{SS} = AGND		0.75	0.825	ms
$t_{ON(Rise)}$	Soft-start time	V_{VCC} = 4.5 V, R_{SS} = 5.76 kΩ		1.5	1.65	ms
$t_{ON(Rise)}$	Soft-start time	V_{VCC} = 4.5 V, R_{SS} = 14 kΩ		3	3.3	ms
$t_{ON(Rise)}$	Soft-start time	V_{VCC} = 4.5 V, R_{SS} = 28.7 kΩ		6	6.6	ms
$t_{ON(Rise)}$	Soft-start time	V_{VCC} = 4.5 V, R_{SS} = open		3	3.3	ms
POWER STAGE						
$R_{DSON(HS)}$	High-side MOSFET on-resistance	T_J = 25°C, PVIN = 12 V, $V_{BOOT\text{-}SW}$ = 4.5 V		4		mΩ
$R_{DSON(HS)}$	High-side MOSFET on-resistance	T_J = 25°C, PVIN = 12 V, $V_{BOOT\text{-}SW}$ = 5.0 V		3.91		mΩ
$R_{DSON(LS)}$	Low-side MOSFET on-resistance	T_J = 25°C, PVIN = 12 V, V_{VDRV} = 4.5 V		1		mΩ
$R_{DSON(LS)}$	Low-side MOSFET on-resistance	T_J = 25°C, PVIN = 12 V, V_{VDRV} = 5 V		0.98		mΩ
$t_{ON(min)}$	Minimum ON pulse width	V_{VCC} = 4.5 V		60		ns
$t_{OFF(min)}$	Minimum OFF pulse width	V_{VCC} = 4.5 V, I_{OUT} = 1.5 A, V_{VOSNS} = $V_{OUT\_Setting}$ – 20 mV, SW falling edge to rising edge		210	250	ns
BOOT CIRCUIT						
$I_{BOOT(LKG)}$	BOOT leakage current	V_{EN} = 2 V, $V_{BOOT\text{-}SW}$ = 5 V			150	µA
$V_{BOOT\text{-}SW(UV\_F)}$	BOOT-SW UVLO falling threshold		2.60	2.76		V
OVERCURRENT LIMIT						
$I_{LS(OCL)}$	Low-side valley overcurrent limit	Valley current limit on LS FET, R_{ILIM} = 7.5 kΩ	11	13	15	A

5.5 Electrical Characteristics (continued)

T_J = –40°C to +125°C. PVIN = 4 V to 16 V, V_{VCC} = 4.5 V to 5.0 V (unless otherwise noted). Typical values are at T_J = 25°C, PVIN = 12 V and V_{VCC} = 4.5 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{LS(OCL)}$	Low-side valley overcurrent limit	Valley current limit on LS FET, R_{ILIM} = 12.1 kΩ	18	20	22	A
$I_{LS(OCL)}$	Low-side valley overcurrent limit	Valley current limit on LS FET, R_{ILIM} = 16.2 kΩ	24.3	27	29.7	A
$I_{LS(OCL)}$	Low-side valley overcurrent limit	Valley current limit on LS FET, R_{ILIM} = 21.5 kΩ	31.5	35	38.5	A
$I_{LS(OCL)}$	Low-side valley overcurrent limit	Valley current limit on LS FET, R_{ILIM} = 24.9 kΩ	36.9	41	45.1	A
$I_{LS(NOC)}$	Low-side negative overcurrent limit	Sinking current limit on LS FET	–18	–16	–14	A
I_{ZC}	Zero-cross detection current threshold	ZC comparator threshold, enter DCM. PVIN = 12 V, V_{VCC} = 4.5 V		1200		mA
	Response delay before entering Hiccup			16	20	µs
	Hiccup sleep time before a restart		49	56	59	ms
OUTPUT OVP AND UVP						
V_{OVF}	V_{OUT} Overvoltage-protection (OVP) threshold	(V_{FB} – V_{GOSNS}) and rising	118.33%	125%	130%	
	OVF response delay	From OVF detection to the start of the NOC operation		100		ns
V_{UVF}	V_{OUT} Undervoltage-protection (UVP) threshold	(V_{FB} – V_{GOSNS}) and falling	60%	66.67%	73.33%	
	UVF response delay	From UVF detection to tri-state of the power FETs		16	20	µs

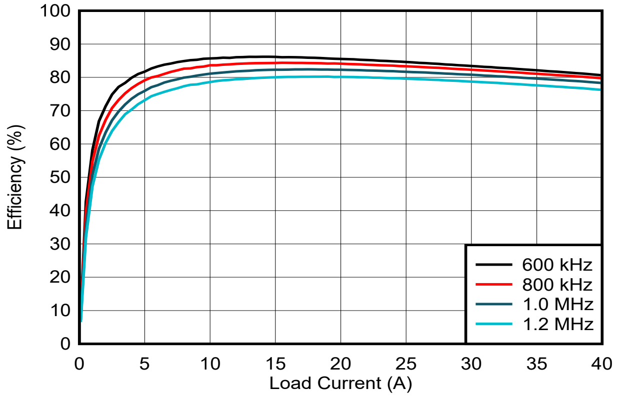
5.5 Electrical Characteristics (continued)

T_J = –40°C to +125°C. PVIN = 4 V to 16 V, V_{VCC} = 4.5 V to 5.0 V (unless otherwise noted). Typical values are at T_J = 25°C, PVIN = 12 V and V_{VCC} = 4.5 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER GOOD						
$V_{OL(PG)}$	PG pin output low-level voltage	I_{PG} = 10 mA, PVIN = 12 V, V_{VCC} = 4.5 V			300	mV
$I_{LKG(PG)}$	PG pin Leakage current when open drain output is high	R_{pullup} = 10 kΩ, V_{PG} = 5 V			5	μA
	Minimum VCC for valid PG pin output	PVIN = 0 V, V_{EN} = 0 V, R_{pullup} = 10 kΩ, $V_{PG} \leq 0.3$ V			1.2	V
OUTPUT DISCHARGE						
	Output discharge on VOSNS pin	PVIN = 12 V, V_{VCC} = 4.5 V, V_{VOSNS} = 0.5 V, EN=0V		455		Ω
THERMAL SHUTDOWN						
$T_{J(SD)}$	Thermal shutdown (Analog OTP) threshold (1)	Junction temperature rising	153	166		°C
$T_{J(HYS)}$	Thermal shutdown (Analog OTP) hysteresis (1)			30		°C

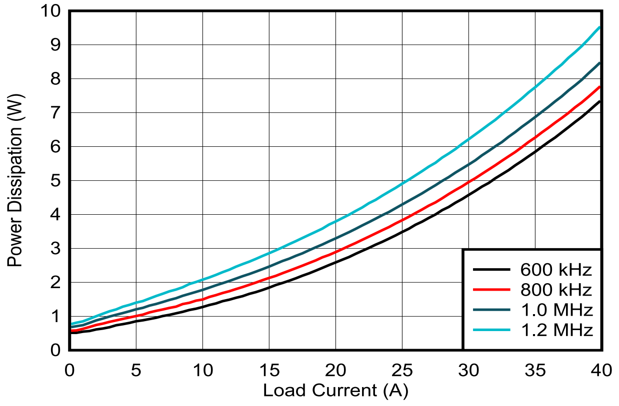
(1) These parameters are provided for reference only, and do not constitute part of TI's published device specifications for purpose of TI's product warranty.

5.6 Typical Characteristics



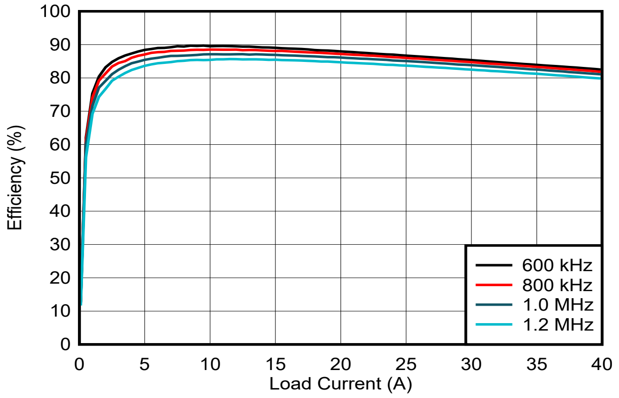
PVIN = 12V VCC = Internal LDO V_{OUT} = 0.76V
MODE = FCCM

Figure 5-1. Efficiency vs Output Current



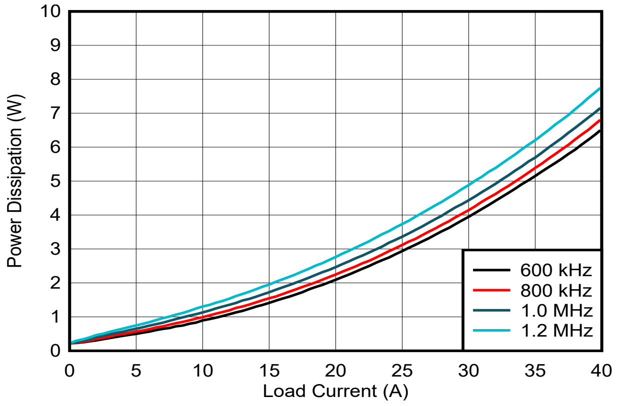
PVIN = 12V VCC = Internal LDO V_{OUT} = 0.76V
MODE = FCCM

Figure 5-2. Power Dissipation vs Output Current



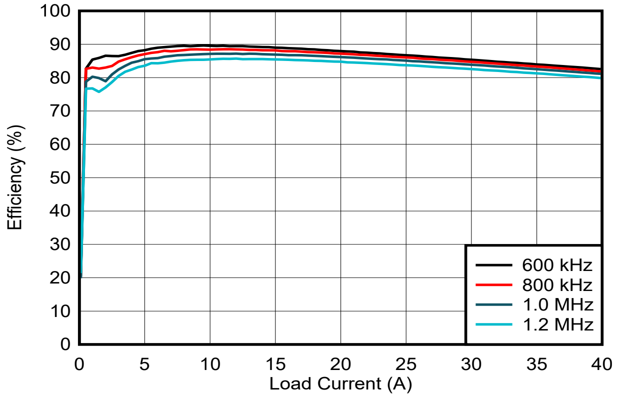
PVIN = 12V VCC = External 5V Bias V_{OUT} = 0.76V
MODE = FCCM

Figure 5-3. Efficiency vs Output Current



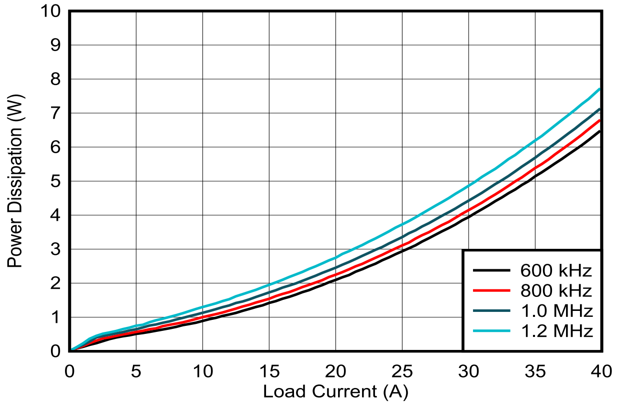
PVIN = 12V VCC = External 5V Bias V_{OUT} = 0.76V
MODE = FCCM

Figure 5-4. Power Dissipation vs Output Current



PVIN = 12V VCC = External 5V Bias V_{OUT} = 0.76V
MODE = DCM

Figure 5-5. Efficiency vs Output Current



PVIN = 12V VCC = External 5V Bias V_{OUT} = 0.76V
MODE = DCM

Figure 5-6. Power Dissipation vs Output Current

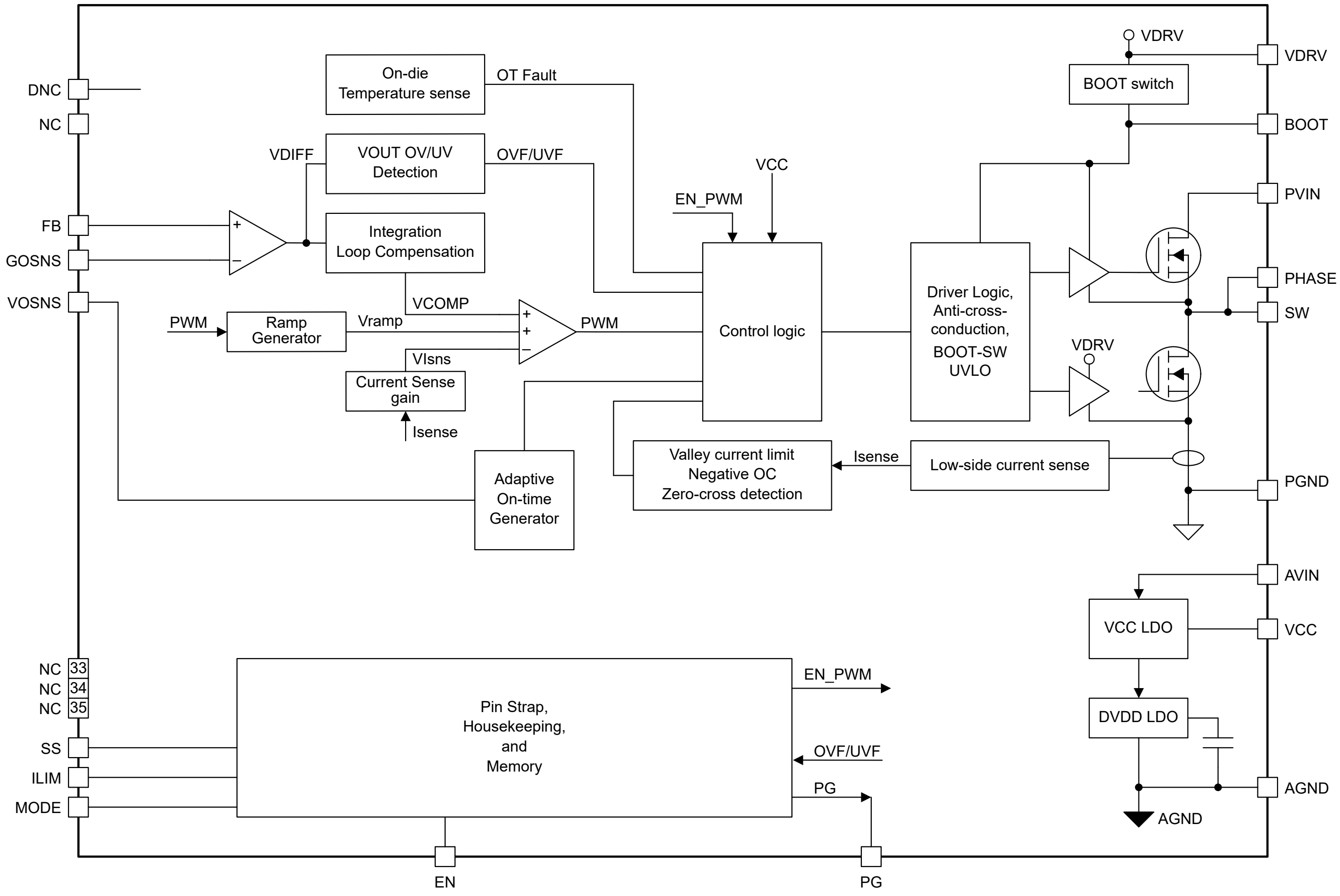
6 Detailed Description

6.1 Overview

The TPS548D26 device is highly integrated buck converter. The device uses D-CAP+ control topology for fast transient response, and accurate load and line regulation. The device is well-designed for space-constrained applications such as data center applications, hardware accelerator, server and cloud computing POLs. The device is easy to use and requires only a few external components.

The TPS548D26 has low RDS_{ON} and supported external 5-V bias to provide high efficiency up to 40 A of continuous current operation. The device has true differential remote sense through VOSNS and GOSNS pins, and an accurate ±1%, with 0.6-V reference over the full operating junction temperature range. The device uses selectable pin strap internal loop compensation. There is no external compensation required. The device provides flexibility to select skip-mode or FCCM operation and programmable soft-start time. The device supports overcurrent, overvoltage, undervoltage, and overtemperature protections TPS548D26 is a lead-free device. The device is fully RoHS compliant without exemption.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Internal VCC LDO and Using an External Bias on the VCC and VDRV Pin

The TPS548D26 device has an internal 4.5-V LDO featuring input from the AVIN pin and output to the VCC pin. When the AVIN voltage rises, the internal LDO is enabled automatically and starts regulating the LDO output voltage on the VCC pin. The VCC voltage provides the bias voltage for the internal analog circuitry on the controller side, and the VDRV voltage provides the supply voltage for the power stage side.

Either the VCC or VDRV pin must be bypassed with a 2.2-µF, at least 6.3-V rating ceramic capacitor. Connecting the VCC pin decoupling capacitor to AGND is required to provide a clean ground for the analog circuitry on the controller side. Referring the VDRV pin decoupling capacitor to PGND is required to minimize the parasitic loop inductance for the driver circuitry in the power stage. Placing a 1-Ω resistor between the VCC pin and VDRV pin forms a RC filter on VCC pin, which greatly reduces the noise impact from power stage driver circuit.

An external bias ranging from 4.75 V to 5.30 V can be connected to the VDRV and VCC pin and power the IC. This action enhances the efficiency of the converter because the VCC and VDRV power supply current now runs off this external bias instead of the internal linear regulator.

A VDRV UVLO circuit monitors the VDRV pin voltage and disables the switching when the VDRV voltage level falls below the VDRV UVLO falling threshold. Maintaining a stable and clean VDRV voltage is required for a smooth operation of the device.

Considerations when using an external bias on the VDRV and VCC pin are shown below:

- Connect the external bias to VDRV pin directly. Place a 1-Ω resistor between the VCC pin and VDRV pin, then VCC is powered through the 1-Ω filtering resistor.
- For a configuration that the VCC pin and AVIN pin are shorted together, the internal LDO is always forced off. A valid external bias is required to be connected to VDRV pin (VCC pin and AVIN pin are also powered by the same external bias through the 1-Ω filtering resistor) so that the internal analog circuits have a stable power supply rail at the power enable.
- For a configuration that the AVIN pin is not shorted to VCC pin, when the external bias is applied on the VDRV pin earlier than AVIN rail (VCC pin is also powered by the same external bias through the 1-Ω filtering resistor), the internal LDO is always forced off and the internal analog circuits have a stable power supply rail at the power enable.
- The VCC and VDRV pins must be powered by the same source, either the internal VCC LDO, or the same external bias.
- (Not recommended) When the external bias is applied on the VDRV pin late (for example, after AVIN rail ramp-up), any power-up and power-down sequencing can be applied as long as there is no excess current pulled out of the VCC pin. Understand that an external discharge path on the VCC or VDRV pin, which can pull a current higher than the current limit of the internal LDO, can potentially turn off VCC LDO thereby shutting off the converter output.
- A good configuration is: Place a 1-Ω resistor between the VCC pin and VDRV pin, and shorting the AVIN pin to VCC pin.
- A good power-up sequence with above configuration is: the external 5-V bias is applied to VDRV pin first (VCC pin is also powered by the same external bias through the 1-Ω filtering resistor), then the 12-V bus applied on PVIN pin, and then the EN signal goes high.

6.3.2 Input Undervoltage Lockout (UVLO)

The TPS548D26 device provides four independent UVLO functions for the broadest range of flexibility in start-up control. While only the fixed VCC_OK UVLO is required to enable the internal memory initialization, all four UVLO functions must be met before the switching can be enabled.

6.3.2.1 Fixed VCC_OK UVLO

The TPS548D26 device has an internally fixed UVLO of 3.15 V (typical) on VCC to enable the digital core and initiate power-on reset, including pin strap detection. The off-threshold on VCC is 3.1 V (typical). After VCC level rises above 3.15 V (typical) and stays above 3.1 V (typical), the I^2C communication is enabled.

6.3.2.2 Fixed VDRV UVLO

The TPS548D26 device has an internally fixed UVLO of 3.6 V (typical) on VDRV to enable drivers for power FETs and output voltage conversion. The off-threshold on VDRV is 3.4 V (typical).

6.3.2.3 Fixed PVIN UVLO

A PVIN UVLO circuit monitors the PVIN level and turns of switching when PVIN level is insufficient. When the PVIN pin voltage is lower than the $PVIN_{UVLO}$ falling threshold voltage (typically 2.30 V), the device stops switching and discharges the internal DAC reference. After the PVIN voltage increases beyond the $\text{PVIN}_{\text{UVLO}}$ rising threshold voltage (typically 2.55 V), the device re-initiates the soft start and switches again. This PVIN UVLO is a non-latch protection.

When the internal VCC LDO is used to power the VCC and VDRV pins, the device switching is not gated by this PVIN UVLO. When the PVIN drops below the level of VDRV UVLO falling threshold plus the LDO dropout voltage, the VDRV UVLO is triggered and the switching stops. When PVIN rises, the PVIN level has to rise above the VDRV UVLO rising threshold to enable the switching. This means using the internal VCC LDO does not allow power conversion under ultra-low PVIN condition.

While, power conversion under ultra-low PVIN condition can be enabled with an external 5-V bias on VCC and VDRV pins. This configuration allows power conversion under ultra-low PVIN condition down to 2.7 V, as long as the external bias maintains at a 5-V level to satisfy both the VCC_OK UVLO and the VDRV UVLO.

6.3.2.4 Enable

The TPS548D26 device offers precise enable, disable threshold on the EN pin. The power stage switching is held off until EN pin voltage rises above the logic high threshold (typically 1.2 V). The power stage switching is turned off after EN pin voltage drops below the logic low threshold (typically 1 V).

The EN pin has an internal filter to avoid unexpected ON or OFF due to short glitches. The deglitch time is set to 0.2 µs.

The recommended operating condition for EN pin is up to 5.3 V and the absolute maximum rating is 5.5 V. *Do not* connect the EN pin to PVIN pin directly.

The TPS548D26 device remains disabled state when EN pin floats. The EN pin is internally pulled down to AGND through a 125-kΩ resistor.

6.3.3 Set the Output Voltage

The output voltage is programmed by the FB voltage divider resistors, R_{FB_top} and R_{FB_bot}. Connect R_{FB_top} between the FB pin and the positive node of the load, and connect R_{FB_bot} between the FB pin and GOSNS pin. The recommended R_{FB_bot} value is 10kΩ, ranging from 1kΩ to 20kΩ. Determine R_{FB_top} by using the below equation:

$$R_{FB\_top} = \frac{V_{OUT} - V_{INTREF}}{V_{INTREF}} \times R_{FB\_bot} \tag{1}$$

Where

- V_{OUT} is the desired output voltage in V.
- V_{INTREF} is 0.6V.

To achieve the overall VOUT accuracy, using ±1% or better accuracy resistor for the FB voltage divider is highly recommended.

The output voltage sensed on the VOSNS pin is fed into the internal on-time generation circuitry. TI recommends shorting the VOSNS pin directly to VOUT sense point (that is, where the R_{FB_top} is connected). Adding any resistance higher than 51Ω between VOUT sense point and the VOSNS pin shifts switching frequency higher than the desired setting. Contact Texas Instruments if a resistor has to be placed between VOUT sense point and the VOSNS pin.

6.3.4 Differential Remote Sense and Feedback Divider

The TPS548D26 device offers true differential remote sense function which is implemented between the FB pin and GOSNS pin. The output of the differential remote sense amplifier is internally fed into the control loop and does not come out to a package pin.

Differential remote sense function compensates a potential voltage drop on the PCB traces thus helps maintain VOUT accuracy under steady state operation and load transient event. Connecting the FB voltage divider resistors to the remote location allows sensing the output voltage at a remote location. The connections from FB voltage divider resistors to the remote location must be a pair of PCB traces with at least 12 mil trace width, and must implement Kelvin sensing across a high bypass capacitor of 0.1 µF or higher on the sensing location. The ground connection of the remote sensing signal must be connected to the GOSNS pin. The VOUT connection of the remote sensing signal must be connected to the VOSNS pin and the top feedback resistor R_{FB_top}. To maintain stable output voltage and minimize the ripple, the pair of remote sensing lines must stay away from any noise sources such as inductor and SW node, or high frequency clock lines. TI recommends to shield the pair of remote sensing lines with ground planes above and below.

The recommended GOSNS operating range (refer to AGND pin) is −100 mV to +100 mV. In case of local sense (no remote sensing), short GOSNS pin to AGND.

6.3.5 Start-Up and Shutdown

Start-Up

The start-up sequence includes three sequential periods. During the first period, the device does initialization which includes building up internal LDOs and references, internal memory initialization, pin strap detection, and so forth. The initialization, which is not gated by EN pin voltage, starts as long as VCC pin voltage is above the VCC_OK UVLO rising threshold (3.15-V typical). The length of this period is about 300 µs for the TPS548D26 device. The pin strap detection result is locked in after the initialization is finished and as long as VCC voltage stays above VCC_OK falling threshold. Changing the external resistor value does not affect the existing pin strap detection result unless the IC is power cycled.

After the EN pin voltage crosses above EN high threshold (typically 1.2 V) the device moves to the second period, power-on delay. The power-on delay is 0.5 ms to activate the control loop and the driver circuit.

The V_{OUT} soft start is the third period. A soft-start ramp, which is an internal signal, starts right after the power-on delay. When starting up without prebias on the output, the internal reference ramps up from 0 V to 0.6 V, and the VOUT ramps up from 0 V to the setting value (by FB voltage divider). A proper soft-start time helps to avoid the inrush current by the output capacitor charging, and also minimize VOUT overshoot. The soft-start time can be selected among 4 options of 0.75 ms, 1.5 ms, 3 ms, and 6 ms by connecting a resistor from pin 29 SS to AGND. Table 6-1 lists the resistor values and the corresponding soft-start time. TI recommends ±1% tolerance resistors with a typical temperature coefficient of ±100 ppm/°C.

For the start-up with a prebiased output, the device limits the discharge current from the prebiased output voltage by preventing the low-side FET from forcing the SW node low until after the first PWM pulse turns on the high-side FET. After the increasing reference voltage exceeds the feedback voltage, which is divided down from the prebiased output voltage, the SW pulses start. This action enables a smooth start-up with a prebiased output.

After VOUT reaches the regulation value, a 1-ms PG delay starts. The converter then asserts PG pin when the 1-ms PG delay expires.

Table 6-1. SS Pin Strap for the Soft-start Time, Fault Response, and Internal Compensation

SS Pin to AGND Resistor (kΩ)	Soft-Start Time (ms)	Internal Compensation	VOUT OV, UV Fault Response
0	0.75	Compensation1	Latch-off
1.50	1.5		
2.49	3		
3.48	6		
4.53	0.75	Compensation2	
5.76	1.5		
7.32	3		
8.87	6		

Table 6-1. SS Pin Strap for the Soft-start Time, Fault Response, and Internal Compensation (continued)

SS Pin to AGND Resistor (kΩ)	Soft-Start Time (ms)	Internal Compensation	VOUT OV, UV Fault Response
10.5	0.75	Compensation1	Hiccup
12.1	1.5		
14.0	3		
16.2	6		
18.7	0.75	Compensation2	
21.5	1.5		
24.9	3		
28.7	6		
Floating	3	Compensation1	Latch-off

Note

The pin strap detection happens at the first stage of power-up sequence. After the detection finishes, the detection results are latched in and do *not* change during the following operation. If a new selection is desired, toggling VCC (or AVIN) is required. Toggling the EN pin does not affect the pin strap detection results.

Shutdown

The TPS548D26 device features a simple shutdown sequence. Both high-side and low-side FET drivers are turned off immediately at the time when the EN pin is pulled low, and the output voltage discharge slew rate is controlled by the external load. The internal reference is discharged down to zero to get ready for the next soft start.

6.3.6 Loop Compensation

The TPS548D26 device features D-CAP+ control topology with internal loop compensation for fast transient response. As listed in Table 6-1, two sets of loop compensation are provided for selecting the AC response to load transients. *Compensation1* provides a mid-band FB to Inductor Current transconductance of 400S and an integrator zero of 10kHz for applications with less strict compensation requirements and using smaller output capacitors. *Compensation2* provides a mid-band FB to Inductor Current transconductance of 1000S and an integrator zero of 2kHz for designs requiring strict transient performance or more output capacitance. *Compensation2* of the TPS548D26 is different than *Compensation2* of the TPS548C26.

Compensation1 provides a dynamic output impedance of 2.5mOhm × Vout/Vref and a minimum recommended L-C resonance of 5kOhms.

Compensation2 provides a dynamic output impedance of 1mOhm × Vout/Vref and a minimum recommended L-C resonance of 1kOhm.

With either compensation, sufficient output capacitance must be provided such that the output impedance is equal to or less than the dynamic impedance of the selected compensation by no more than ½ of the switching frequency.

To avoid wrong pin strap detection, TI recommends ±1% tolerance resistors with a typical temperature coefficient of ±100 ppm/°C.

Using a Feedfoward Capacitor

Adding a feedforward capacitor to the VOUT to FB divider can reduce the Vout/Vref factor to reduce the dynamic output impedance, but require additional output capacitance. The maximum reduction is 2.5mOhms for Compensation1 and 1mOhm for Compensation2. The exact reduction depends on the impedance divider ratio R1//C1:R2 at the frequency when the output capacitor impedance matches the dynamic impedance.

6.3.7 Set Switching Frequency and Operation Mode

TPS548D26 device provides programmable operation mode including the forced CCM operation for tight output voltage ripple and auto-skipping Eco-mode for high light-load efficiency. The TPS548D26 device allows users to select the switching frequency and operation mode through the pin strap detection on MODE pin. Table 6-2 lists the resistor values for the switching frequency and operation mode selections. TI recommends ±1% tolerance resistors with a typical temperature coefficient of ±100 ppm/°C.

The FCCM bit is set during initial power-on and latched after the power conversion is enabled (EN=high). While the device is enabled, a write to FCCM bit is acknowledged but the operation mode does not change until an EN toggle happens.

Table 6-2. MODE Pin Strap for Switching Frequency and Operation MODE

MODE Pin to AGND Resistor (kΩ)	Switching Frequency (kHz)	Operation Mode
0	600	FCCM
1.50	800	
2.49	1000	
3.48	1200	
10.5	600	Auto-skipping Eco-mode (DCM)
12.1	800	
14	1000	
16.2	1200	
Floating	800	FCCM

Note

The pin strap detection happens at the first stage of power-up sequence. After the detection finishes, the detection results are latched in and do *not* change during the following operation. If a new selection is desired, toggling VCC (or AVIN) is required. Toggling the EN pin does not affect the pin strap detection results.

6.3.8 Switching Node (SW)

The SW pins connect to the switching node of the power conversion stage. The SW pins act as the return path for the high-side gate driver. During nominal operation, the voltage swing on SW normally traverses from below ground to above the input voltage. Parasitic inductance in the PVIN to PGND loop (including the component from the PCB layout and also the component inside the package) and the output capacitance (COSS) of both power FETs form a resonant circuit that can produce high frequency (> 100 MHz) ringing on this node. The voltage peak of this ringing, if not controlled, can be significantly higher than the input voltage. TPS548D26 high-side gate driver is fine tuned to minimize the peak ringing amplitude so that a RC snubber on SW node is usually not needed. However, TI highly recommends for the user to measure the voltage stress across either the high-side or low-side FET and make sure that the peak ringing amplitude does not exceed the absolute maximum rating limit listed in the *Absolute Maximum Ratings* table.

6.3.9 Overcurrent Limit and Low-side Current Sense

For a synchronous buck converter, the inductor current increases at a linear rate determined by the input voltage, the output voltage, and the output inductor value during the high-side MOSFET on-time (ON time). During the low-side MOSFET on-time (OFF time), this inductor current decreases linearly per slew rate determined by the output voltage and the output inductor value. The inductor during the OFF time, even with a negative slew rate, usually flows from the device SW node to the load the device which is said to be sourcing current and the output current is declared to be positive. This section describes the overcurrent limit feature based on the positive low-side current. The next section describes the overcurrent limit feature based on the negative low-side current.

The positive overcurrent limit (OCL) feature in the TPS548D26 device is implemented to clamp low-side *valley current* on a cycle-by-cycle basis. The inductor current is monitored during the OFF time by sensing the current flowing through the low-side MOSFET. When the sensed low-side MOSFET current remains above the selected OCL threshold, the low-side MOSFET stays ON until the sensed current level becomes lower than the selected OCL threshold. This operation extends the OFF time and pushes the next ON time (where the high-side MOSFET turns on) out. As a result, the average output current sourced by the device is reduced. As long as the load pulls a heavy load where the sensed low-side *valley current* exceeds the selected OCL threshold, the device continuously operates in this clamping mode which extends the current OFF time and pushes the next ON time out. The device does not implement a fault response circuit directly tied to the overcurrent limit circuit, instead, the VOUT UVF function is used to shuts the device down under an overcurrent fault.

During an overcurrent event, the current sunk by the load (I_{OUT}) exceeds the current sourced by the device to the output capacitors, thus, the output voltage tends to decrease. Eventually, when the output voltage falls below the selected undervoltage fault threshold, the VOUT UVF comparator detects and shuts down the device after the UVF Response Delay (typically 16µs). The device then responds to the VOUT UVF trigger per fault response selected through SS pin. With the *Latch-off* response selected, the device latches OFF both high-side and low-side drivers. The latch is cleared with a reset of VCC or by toggling the EN pin. With the *Hiccup* response selected, the device enters hiccup mode and restarts automatically after a hiccup sleep time of 56ms, without limitation on the number of restart attempts. In other words, the response to an overcurrent fault is set by the selected UVF response.

If an OCL condition happens during a soft-start ramp, the device still operates with the cycle-by-cycle current limit based on the sensed low-side valley current. This operation can limit the energy charged into the output capacitors thus the output voltage likely ramps up slower than the desired soft-start slew rate. During the soft start, the VOUT UVF comparator is disabled, thus the device does not respond to an UVF event. Upon the completion of the soft start, the VOUT UVF comparator is enabled, then the device starts responding to the UVF event.

The resistor, R_{ILIM}, connected from the ILIM pin to AGND sets the overcurrent limit threshold (see the following table). TI recommends ±1% tolerance resistors with a typical temperature coefficient of ±100 ppm/°C.

Table 6-3. ILIM Pin Strap for Overcurrent Limit Threshold

ILIM Pin to AGND Resistor (kΩ)	OCL Threshold (Valley Current Detection)
7.5	13A
12.1	20A
16.2	27A
21.5	35A
24.9	41A

Note

The pin strap detection happens at the first stage of power-up sequence. After the detection finishes, the detection results are latched in and do *not* change during the following operation. If a new selection is desired, toggling VCC (or AVIN) is required. Toggling the EN pin does not affect the pin strap detection results.

6.3.10 Negative Overcurrent Limit

The TPS548D26 device is a synchronous buck converter, thus the current can flow from the device to the load or from the load into the device through SW node. When the current is flowing from the device SW node to the load the device is said to be sourcing current and the output current declared to be positive. When the current is flowing into the device SW node from the load, the device is said to be sinking current and the current is declared to be negative.

The device offers a fixed, cycle-by-cycle negative overcurrent (NOC) limit which is set to −16 A. Similar with the positive overcurrent limit, the inductor current is monitored during the low-side FET on period. To prevent too large of a negative current and a damage of low-side FET, the device turns off the low-side FET after the detected negative current through the low-side FET exceeds the NOC limit. And then the high-side FET is turned on for an on-time determined by PVIN, VOUT, and f_{SW} setting. After the high-side FET on-time expires, the low-side FET turns on again.

The device is unlikely to trigger the −16-A negative current limit during the nominal operation unless too small of an inductor value is chosen or the inductor becomes saturated. This NOC operation feature is used to discharge output capacitors during an overvoltage event.

6.3.11 Zero-Crossing Detection

TPS548D26 device implements an internal circuit for the zero inductor-current detection during skip-mode operation. The fixed Z-C detection threshold is set to a slightly positive value such as 300 mA to compensate the delay time of the Z-C detection circuit and avoid too-late detection. Depending on the inductor value, frequency, VIN and Vout conditions, this can result diode conduction for a short period.

6.3.12 Input Overvoltage Protection

The TPS548D26 device actively monitors the PVIN input voltage. When the PVIN voltage level is above the input overvoltage threshold, TPS548D26 device stops switching and pulls PG signal low. The PVIN OV rising threshold is typically 18.6 V while the PVIN OV falling threshold is typically 13.4 V.

After the PVIN overvoltage fault is triggered, the device latches off both the high-side and low-side FETs until the EN pin is toggled or PVIN is reset.

6.3.13 Output Undervoltage and Overvoltage Protection

The TPS548D26 device monitors the FB node voltage (V_{FB} − V_{GOSNS}) to provide overvoltage (OV) and undervoltage (UV) protection.

VOUT UVF

When the FB node voltage (V_{FB} − V_{GOSNS}) drops to 400mV or lower, the UVF comparator detects and an internal UVF Response Delay counter begins. When the 16µs UVF Response Delay expires, the device responds per the fault response selected through the SS pin. With the *Latch-off* response selected, the device latches OFF both high-side and low-side FETs. The latch is cleared with a reset of VCC or by toggling the EN pin. With the *Hiccup* response selected, the device enters hiccup mode and restarts automatically after a hiccup sleep time of 56ms, without limitation on the number of restart attempts.

The UVF function is enabled only after the soft-start period completes.

During the UVF Response Delay, if the FB node voltage (V_{FB} − V_{GOSNS}) rises above the UVF threshold, thus not qualified for a UVF event, the UVF response delay timer resets to zero. When the VOUT drops below the UVF threshold again, the UVF response delay timer restarts from zero.

VOUT OVF

When the FB node voltage (V_{FB} − V_{GOSNS}) rises to 750mV or higher, the OVF comparator detects and the device immediately latches OFF the high-side FET and turns on the low-side FET until the current flowing through low-side FET exceeds the negative overcurrent (NOC) limit. Upon reaching the −16A NOC limit, the low-side FET is turned off, and the high-side FET is turned on again for an on-time determined by PVIN, VOUT, and f_{SW} setting. The device operates in this cycle until the output voltage is fully discharged. After VOUT is fully discharged, the high-side FET is latched OFF and the low-side FET is latched ON. With the *Latch-off* response selected, the device is kept under the state of the high-side FET latched OFF and the low-side FET latched ON. The latch is cleared with a reset of VCC or by toggling the EN pin. With the *Hiccup* response selected, the device still discharges output voltage by running the NOC operation. However, the device re-starts automatically after a hiccup sleep time of 56ms, without limitation on the number of restart attempts. The hiccup sleep time counter starts right after the OVF trigger.

The OVF function is enabled only after the soft-start period completes.

6.3.14 Overtemperature Protection

To have full coverage for a potential overtemperature event, the TPS548D26 device implements two overtemperature protection circuitries - one on the Controller side and one on the Power Stage (PS) side.

OTP by Monitoring the Power Stage Temperature

A temperature sensing circuit is implemented in the Power Stage (PS) side. This sensed temperature is fed into an OTP circuit on the PS side to be compared with a fixed threshold (rising 166°C typical). The device stops the SW switching when the sensed IC temperature goes beyond the fixed threshold. After the PS die temperature falls 30°C below the rising threshold, the device automatically restarts with an initiated soft start. This OTP on power stage side is a non-latch protection.

OTP by Monitoring the Controller Temperature

The Controller features an internal on-die temperature sensing circuit. The sensed temperature signal is fed into an OTP comparator on the Controller side and compared with a fixed threshold (rising 166°C typical). The device stops the SW switching when the sensed Controller temperature goes beyond the fixed threshold. The device response to an OTP event is set by the SS pin strap detection. With the *Latch-off* response selected, the device latches OFF both high-side and low-side FETs. The latch is cleared with a reset of VCC or by toggling the EN pin. With the *Hiccup* response selected, the device enters hiccup mode and re-starts automatically after a hiccup sleep time of 56 ms, without limitation on the number of restart attempts.

Given the power loss on the controller side is much less than the power loss on the power stage side, the OTP on controller side is unlikely to trigger during the nominal operation.

6.3.15 Power Good

The TPS548D26 device offers a power-good output on PG pin, which asserts high when the converter output is within the target. The PG output stays low when the switching is disabled by EN pin or insufficient PVIN level. The PG output is an open-drain output and must be pulled up externally through a pullup resistor (usually 10 kΩ). The recommended PG pullup resistor value is from 1 kΩ to 100 kΩ.

The PG function is activated after VCC voltage level reaches the minimum VCC threshold for a valid PG output (maximum 1.2 V). When VCC is lower than 1.2 V, the PG circuit does not have sufficient power supply and the open-drain output is always high-Z. The power-good function is fully activated after the soft-start ramp is completed and the 1 ms PG delay expires.

6.4 Device Functional Modes

6.4.1 Forced Continuous-Conduction Mode

When the operation mode is set to FCCM, the controller operates in continuous conduction mode (CCM) during light-load conditions. During CCM, the switching frequency maintained to an almost constant level over the entire load range which is suitable for applications requiring tight control of the switching frequency at the cost of lower efficiency.

When FCCM is selected, the TPS548D26 device operates at CCM during the whole soft-start period as well as the nominal operation.

6.4.2 Auto-Skip Eco-mode Light Load Operation

When the operation mode is set to DCM, the device automatically reduces the switching frequency at light-load conditions to maintain high efficiency. This section describes the operation in detail.

As the output current decreases from heavy load condition, the inductor current also decreases until the rippled valley of the inductor current touches zero level. Zero level is the boundary between the continuous-conduction and discontinuous-conduction modes. The synchronous MOSFET turns off when this zero inductor current is detected. As the load current decreases further, the converter runs into discontinuous-conduction mode (DCM).

The on-time is maintained to a level approximately the same as during continuous-conduction mode operation so that discharging the output capacitor with a smaller load current to the level of the reference voltage requires more time. Calculate the transition point to the light-load operation IOUT(LL) (for example, the threshold between continuous- and discontinuous-conduction mode) using the following equation.

$$I_{OUT(LL)} = \frac{1}{2 \times L \times f_{SW}} \times \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}} \tag{2}$$

where

- f_{SW} is the switching frequency

TI recommends using low ESR capacitors (such as ceramic capacitor) for skip-mode.

6.4.3 Powering the Device From a 12-V Bus

The device works well when powering from a 12-V bus with a single V_{IN} configuration. As a single V_{IN} configuration, the internal LDO is powered by the 12-V bus and generates 4.5-V output to bias the internal analog circuitry and also powers up the gate drives. The V_{IN} input range under this configuration is 4 V to 16 V for up to 40-A load current. Figure 6-1 shows an example for this single V_{IN} configuration.

V_{IN} and EN are the two signals to enable the part. For start-up sequence, any sequence between the V_{IN} and EN signals can power the device up correctly.

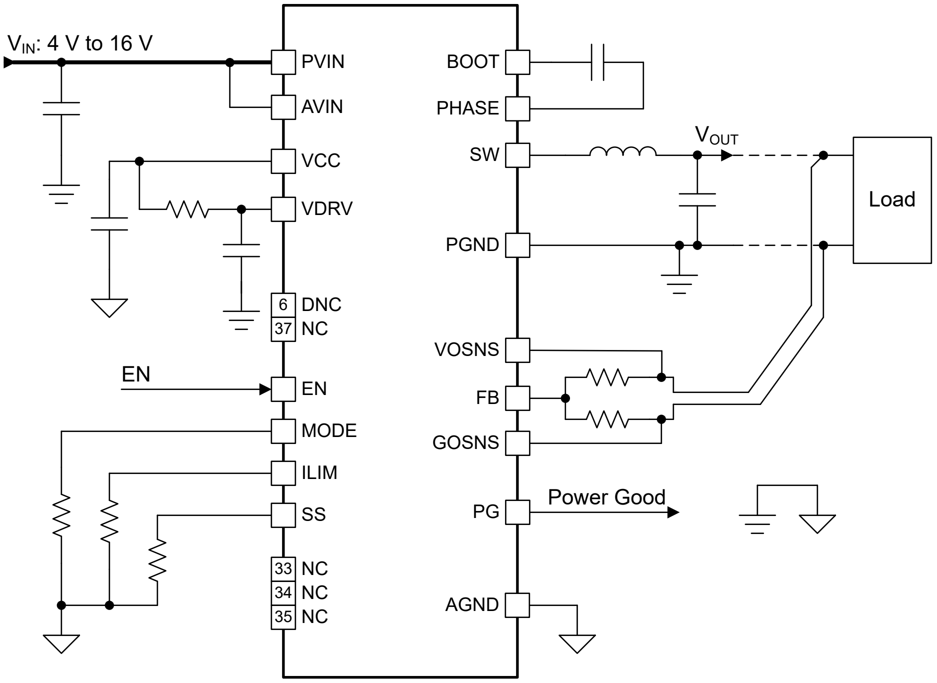


Figure 6-1. Single V_{IN} Configuration With 12-V Bus

6.4.4 Powering the Device From a Split-Rail Configuration

When an external bias that is at a different level from the main V_{IN} bus is applied to the VDRV pin, the device can be configured to split rail by using both the main V_{IN} bus and the VDRV bias. Connecting a valid bias rail to the VDRV pin overrides the internal VCC LDO, saving power loss on that linear regulator. This configuration helps improve overall system-level efficiency but requires a valid VCC bias. A 5.0-V rail is the common choice for the VDRV bias. With a stable VDRV bias, the V_{IN} input range under this configuration can be as low as 2.7 V and up to 16 V.

The noise of the external bias affects the internal analog circuitry. To make sure of a proper operation, a clean, low-noise external bias, and a local decoupling capacitor from the VDRV pin to PGND pin are required. Figure 6-2 shows an example for this split rail configuration.

The VDRV external bias current during nominal operation varies with the bias voltage level and the switching frequency. For example, by setting the device to skip mode, the VDRV pin draws less and less current from the external bias when the switching frequency decreases under light load condition. The typical VDRV external bias current under FCCM operation is listed in the *Electrical Characteristics* table to help the user prepare the capacity of the external bias.

Under split rail configuration, PVIN, VDRV bias, and EN are the signals to enable the part. For the start-up sequence, TI recommends that the external bias is applied on the VDRV pin earlier than PVIN rail. A practical start-up sequence example is the external 5-V bias is applied first, then the 12-V bus is applied on PVIN, and then EN signal goes high.

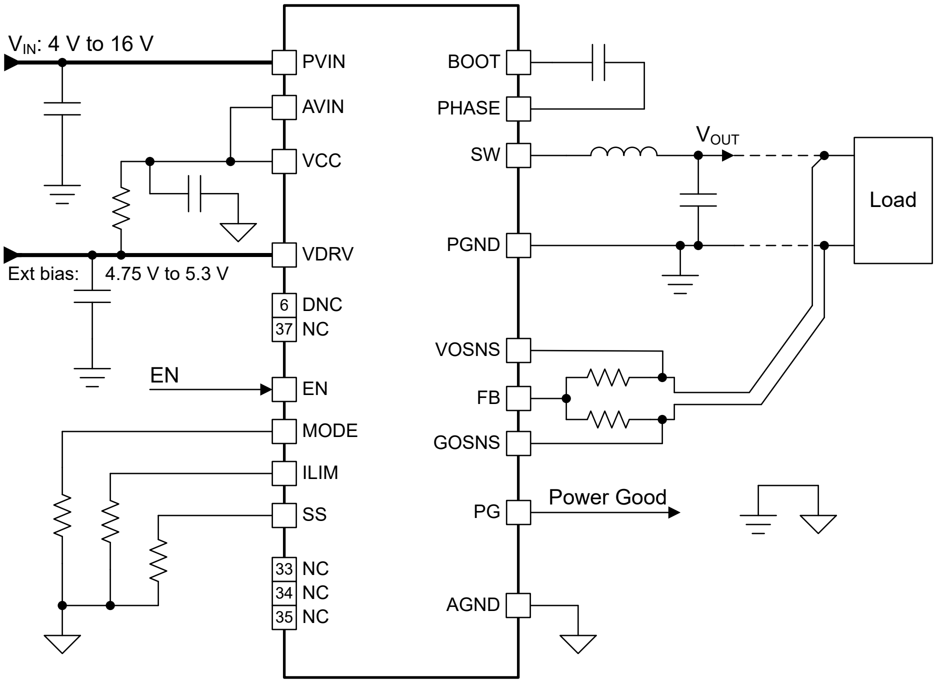


Figure 6-2. Split-Rail Configuration With External VCC Bias

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

The TPS548D26 device is a highly-integrated, synchronous, step-down DC/DC converter. The TPS548D26 has a simple design procedure where programmable parameters can be configured through pin strap detections.

7.2 Typical Application

7.2.1 Application

This design describes a 3.3V, 40A application for the TPS548D26EVM.

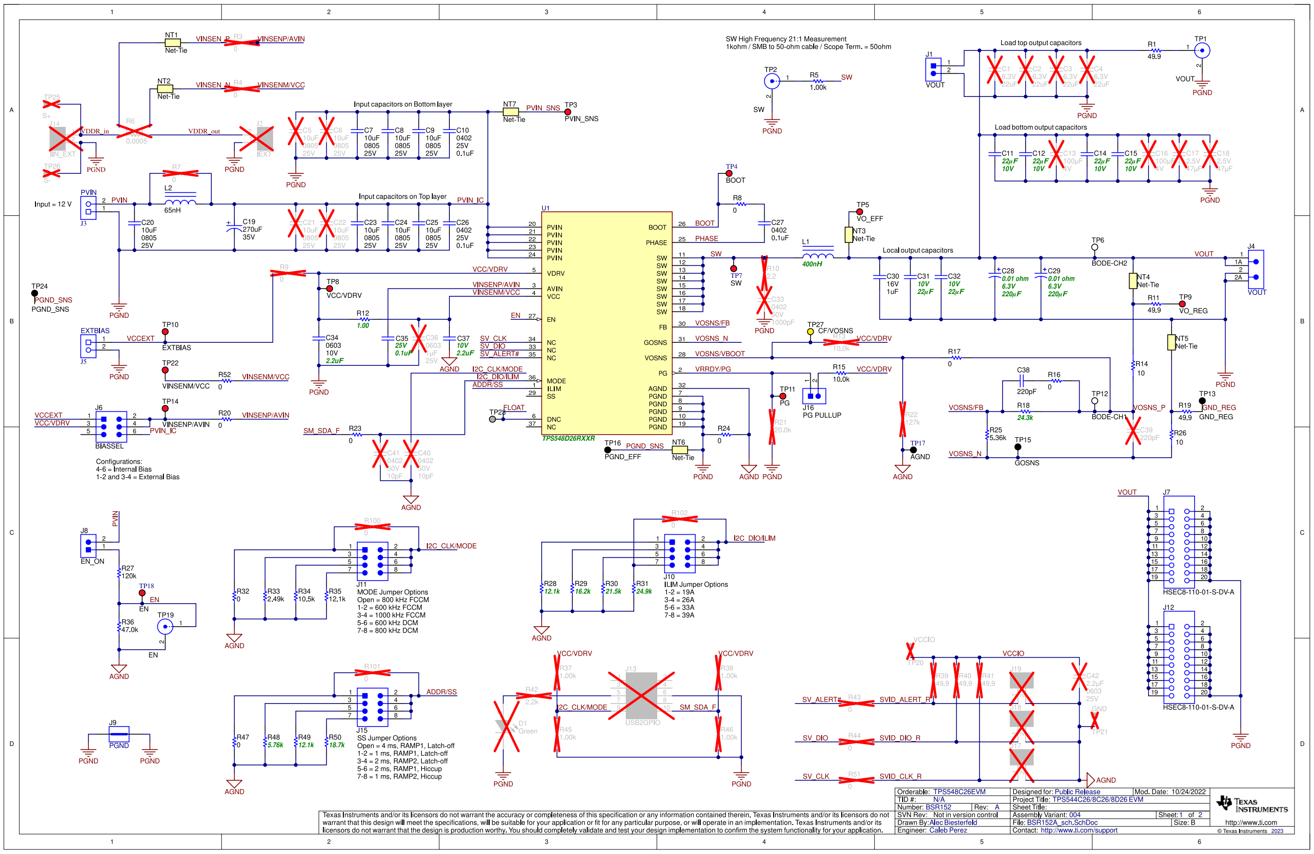


Figure 7-1. TPS548D26EVM 3.3V Output Application

7.2.2 Design Requirements

This design uses the parameters listed in the following table.

Table 7-1. Design Parameters

PARAMETER	VALUE
Input voltage	10.8V – 13.2V
Output voltage	1.1V
Output current	40A
Switching frequency	1000kHz

7.2.3 Detailed Design Procedure

This design example leverages the requirements for the TPS548D26EVM. The default settings for this device are designed for this application. The following steps illustrate how to select key components.

7.2.3.1 Inductor Selection

In general, a smaller inductance increases loop bandwidth leading to better transient response at the expense of higher current and voltage ripple. Select the inductor such that the transient performance and ripple requirements are balanced for a particular design. The recommendation is that the inductor ripple current is kept within the range of 20% to 40% of the desired output current. In this example, a 400nH, 0.8mΩ inductor is used.

7.2.3.2 Input Capacitor Selection

Select input capacitors to provide reduction in input voltage ripple and high-frequency bypassing, which in return reduces switching stress on the power stage MOSFETs internal to the device. In this example, a 0.1-μF, 25-V, 0402 ceramic capacitor must be placed as close as possible to pin 20 of the device on the same layer as the IC on the PCB. In addition, 6pcs 10-μF ceramic capacitors are used and an optional 270-μF bulk capacitor is used on the input.

7.2.3.3 Output Capacitor Selection

To meet the output voltage ripple and load transient requirements, use a 1μF and 2pcs, 22μF ceramic capacitors local to the output of the inductor. Additionally, use 2pcs, 220μF bulk capacitors on the top-side of the PCB combined with 4pcs, 22μF ceramic capacitors on the bottom-side of the PCB.

7.2.3.4 VCC and VRDV Bypass Capacitor

Connect a 2.2-μF, 6.3-V (or 10 V) rated ceramic capacitor to AGND for bypassing of the VCC pin.

Connect a 2.2-μF, 6.3-V (or 10 V) rated ceramic capacitor to PGND for bypassing of the VDRV pin. This bypass capacitor must refer to PGND pin 7 – 10 to minimize the length of high-frequency driving current path.

Placing a 1-Ω resistor between the VCC and VDRV pin forms a RC filter on VCC pin, which greatly reduces the noise impact from power stage driver circuit.

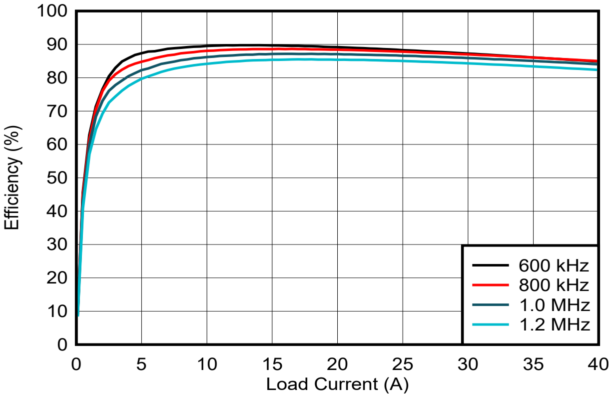
7.2.3.5 BOOT Capacitor Selection

Use a minimum of a 0.1-μF capacitor connected from Phase (pin 25) to Boot (pin 26). An optional series boot resistor of 0 Ω or 2.2 Ω can be added.

7.2.3.6 PG Pullup Resistor Selection

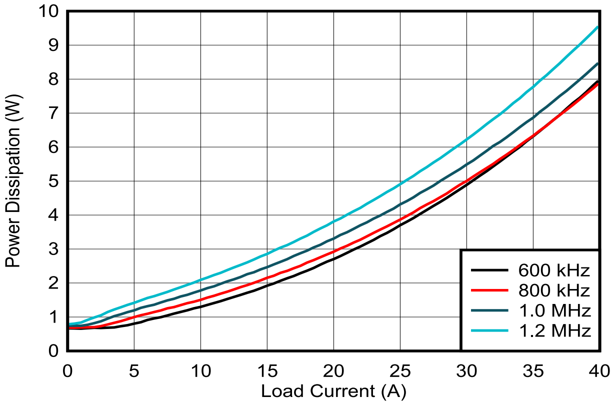
The PG output is an open-drain output and must be pulled up externally through a pullup resistor. Place a pullup resistor, within a 1-kΩ to 100-kΩ range, at the PG pin (pin 2). In this example, PG is pulled up to VCC/VDRV with a 10-kΩ resistor.

7.2.4 Application Curves



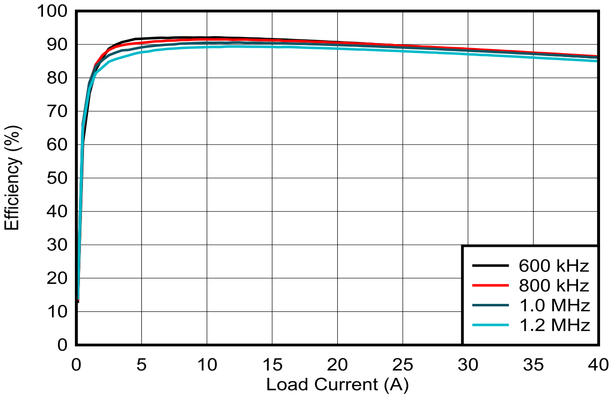
PVIN = 12V
VCC = Internal LDO
V_{OUT} = 1.1V
MODE = FCCM

Figure 7-2. Efficiency vs Output Current



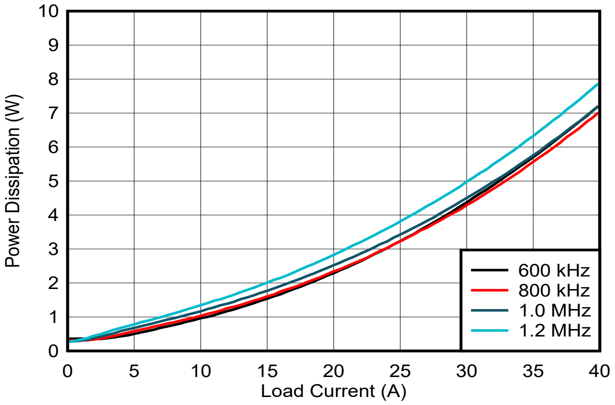
PVIN = 12V
VCC = Internal LDO
V_{OUT} = 1.1V
MODE = FCCM

Figure 7-3. Power Dissipation vs Output Current



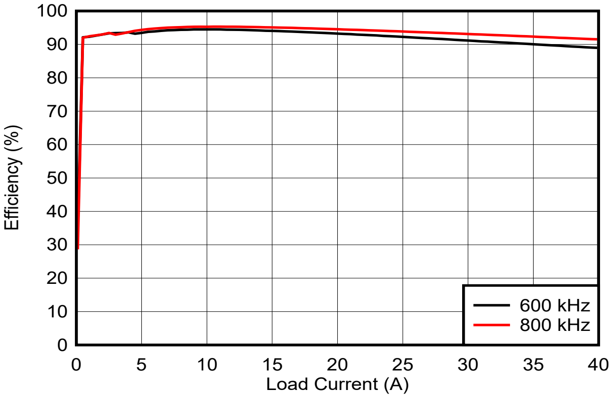
PVIN = 12V
VCC = External 5V Bias
V_{OUT} = 1.1V
MODE = FCCM

Figure 7-4. Efficiency vs Output Current



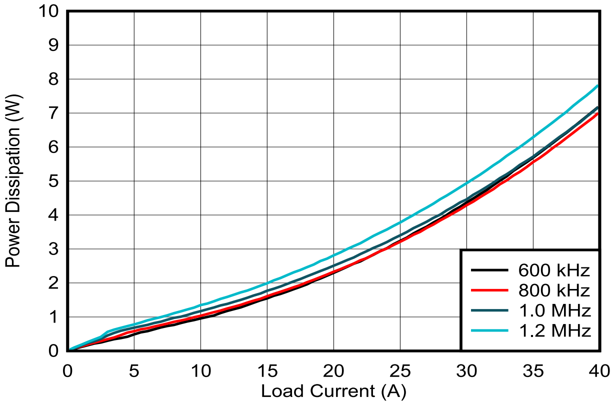
PVIN = 12V
VCC = External 5V Bias
V_{OUT} = 1.1V
MODE = FCCM

Figure 7-5. Power Dissipation vs Output Current



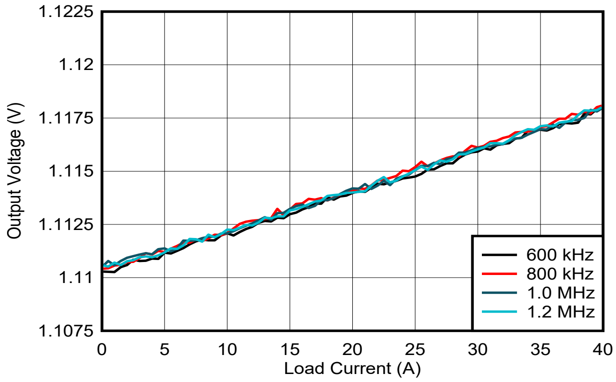
PVIN = 12V
VCC = External 5V Bias
V_{OUT} = 1.1V
MODE = DCM

Figure 7-6. Efficiency vs Output Current



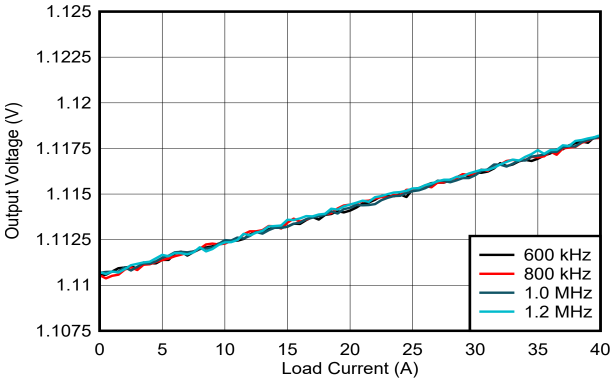
PVIN = 12V
VCC = External 5V Bias
V_{OUT} = 1.1V
MODE = DCM

Figure 7-7. Power Dissipation vs Output Current



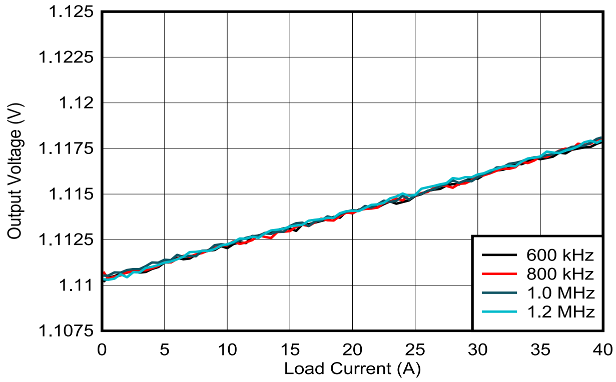
PVIN = 12V
VCC = Internal LDO
V_{OUT} = 1.1V
MODE = FCCM
No DC Load Line (DCLL)

Figure 7-8. Load Regulation vs Output Current



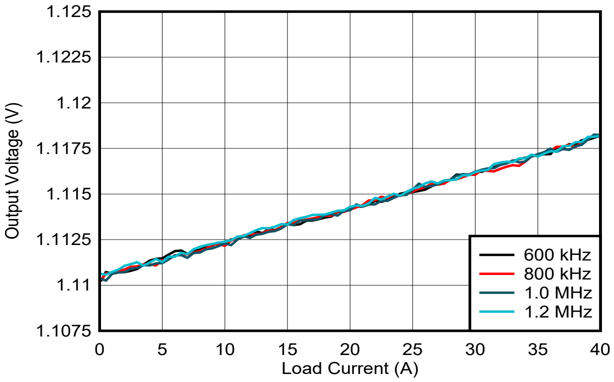
PVIN = 12V
VCC = External 5V Bias
V_{OUT} = 1.1V
MODE = FCCM
No DC Load Line (DCLL)

Figure 7-9. Load Regulation vs Output Current



PVIN = 12V
VCC = Internal LDO
V_{OUT} = 1.1V
MODE = DCM
No DC Load Line (DCLL)

Figure 7-10. Load Regulation vs Output Current



PVIN = 12V
VCC = External 5V Bias
V_{OUT} = 1.1V
MODE = DCM
No DC Load Line (DCLL)

Figure 7-11. Load Regulation vs Output Current

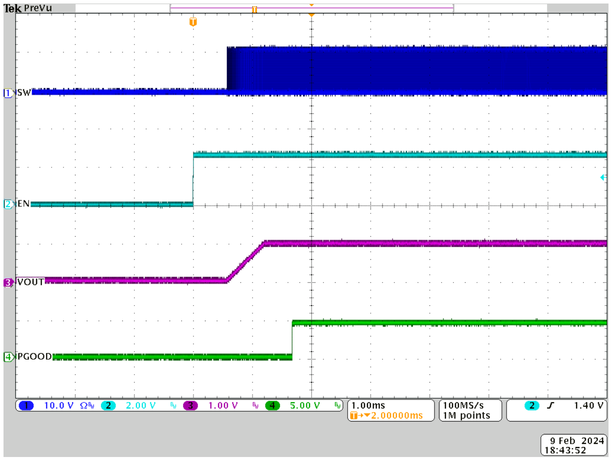


Figure 7-12. ENABLE Start-Up Waveform, PVIN = 12V, VOUT = 1.1V

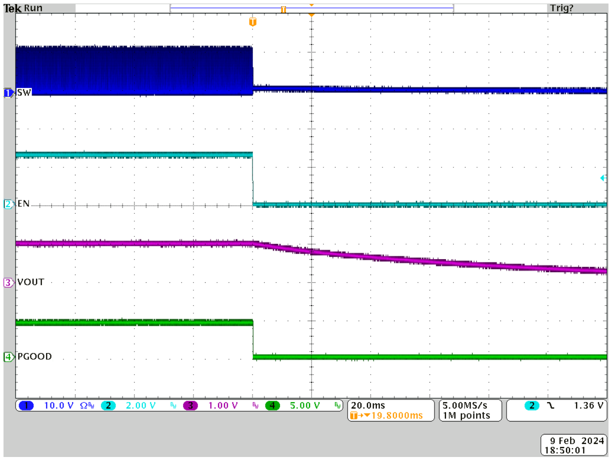
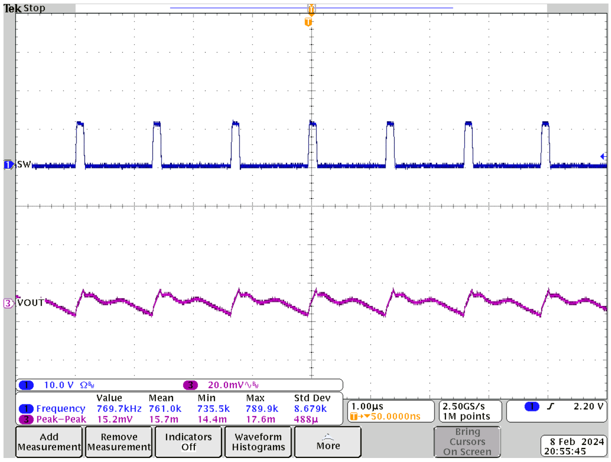
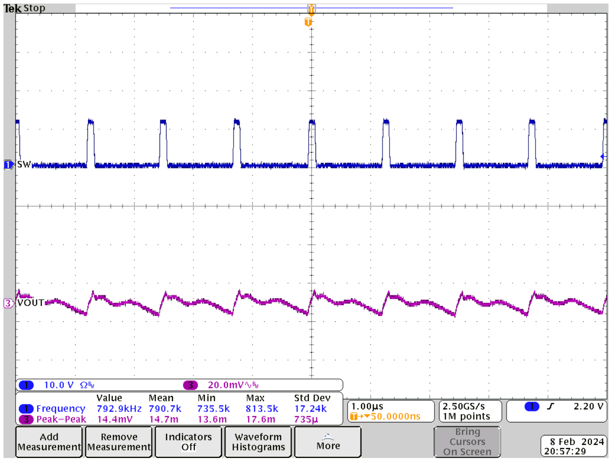


Figure 7-13. ENABLE Shutdown Waveform, PVIN = 12V, VOUT = 1.1V



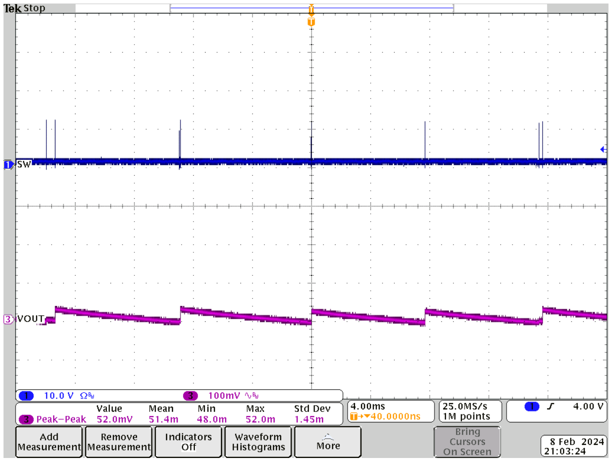
	Value	Mean	Min	Max	Std Dev
1 Frequency	769.7kHz	761.0k	735.5k	789.9k	8.679k
3 Peak–Peak	15.2mV	15.7m	14.4m	17.6m	488µ

Figure 7-14. Output Voltage Ripple, 800kHz FCCM, 40A Load, PVIN = 12V, VOUT = 1.1V



	Value	Mean	Min	Max	Std Dev
1 Frequency	792.9kHz	790.7k	735.5k	813.5k	17.24k
3 Peak–Peak	14.4mV	14.7m	13.6m	17.6m	735µ

Figure 7-15. Output Voltage Ripple, 800kHz FCCM, No load, PVIN = 12V, VOUT = 1.1V



	Value	Mean	Min	Max	Std Dev
3 Peak–Peak	52.0mV	51.4m	48.0m	52.0m	1.45m

Figure 7-16. Output Voltage Ripple, DCM, No load, PVIN = 12V, VOUT = 1.1V

7.3 Power Supply Recommendations

The device is designed to operate from a wide input voltage supply range between 2.7 V and 16 V when the VDRV pin is powered by an external bias ranging from 4.75 V to 5.3 V. Both input supplies (PVIN and VDRV bias) must be well regulated. Proper bypassing of input supplies (PVIN and VDRV) is also critical for noise performance, as are PCB layout and grounding scheme. See the recommendations in *Layout Guidelines*.

7.4 Layout

7.4.1 Layout Guidelines

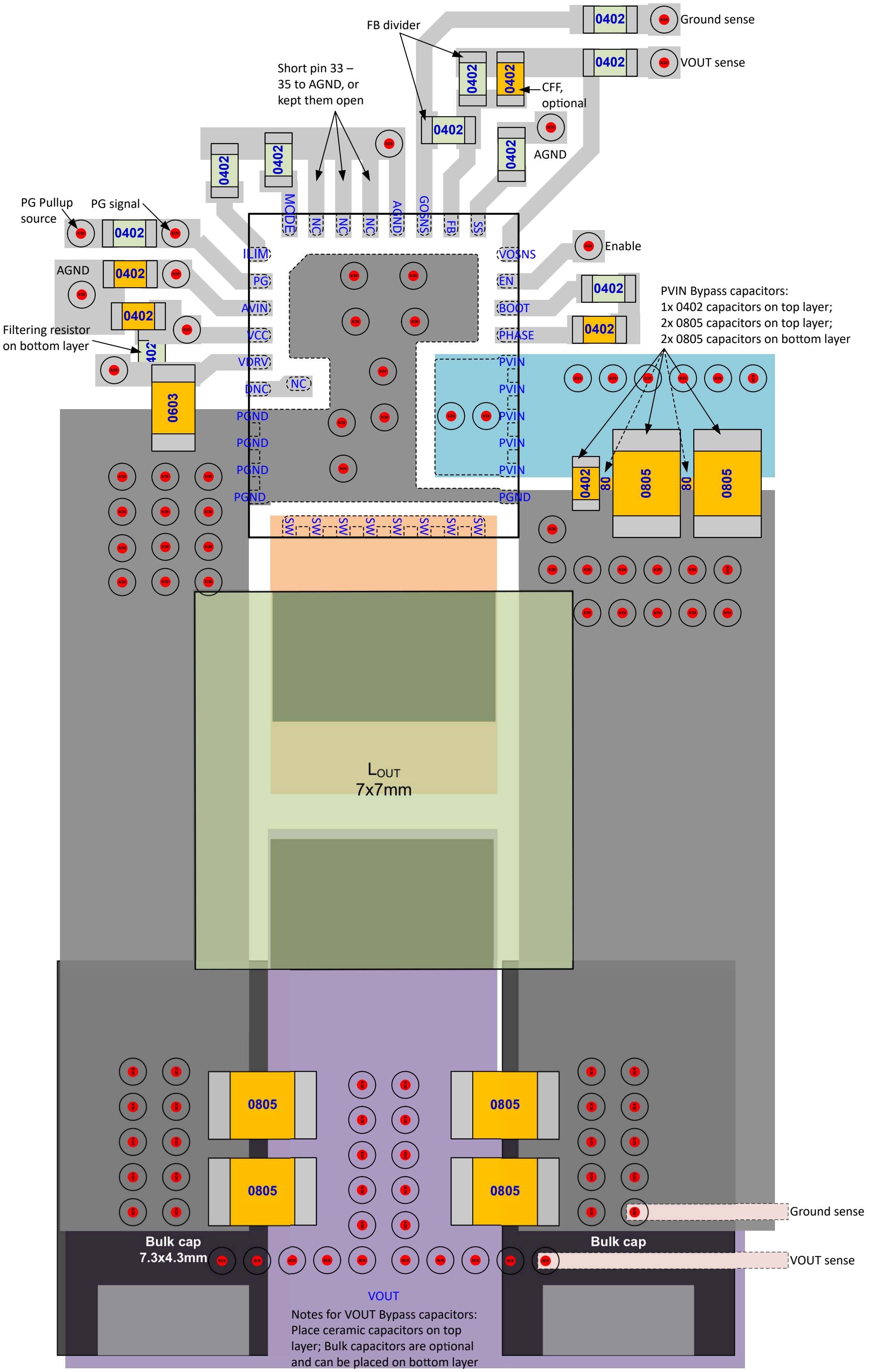
Layout is critical for good power supply design. Layout example shows the recommended PCB layout configuration. A list of PCB layout considerations using the device is listed as follows:

- Place the power components (including input and output capacitors, the inductor, and the IC) on the top side of the PCB. To shield and isolate the small signal traces from noisy power lines, insert at least one solid ground inner plane.
- PVIN-to-PGND decoupling capacitors are important for FET robustness. Besides the large volume 0603 or 0805 ceramic capacitors, TI highly recommends a 0.1-µF, 0402 ceramic capacitor with 25-V / X7R rating on PVIN pin 20 (top layer) to bypass any high frequency current in PVIN to PGND loop. TI recommends the 25-V rating, but can be lowered to 16-V rating for an application with tightly regulated 12-V input bus.
- When one or more PVIN-to-PGND decoupling capacitors are placed on bottom layer, extra impedance is introduced to bypass IC PVIN node to IC PGND node. Placing at least 3 times PVIN vias on PVIN pad

(formed by pin 20 to pin 24) and at least nine times PGND vias on the thermal pad (underneath of the IC) is important to minimize the extra impedance for the bottom layer bypass capacitors.

- Except the PGND vias underneath the thermal pad, place at least four PGND vias as close as possible to the PGND pin 7 to pin 10. Place at least two PGND vias as close as possible to the PGND pin 19. This action minimizes PGND bounces and also lowers thermal resistance.
- Place the VDRV-to-PGND decoupling capacitor as close as possible to the device. TI recommends a 2.2-µF/6.3 V/X7R/0603 or 4.7-µF/6.3 V/X6S/0603 ceramic capacitor. The voltage rating of this bypass capacitor must be at least 6.3 V but no more than 10 V to lower ESR and ESL. The recommended capacitor size is 0603 to minimize the capacitance drop due to DC bias effect. Make sure the VDRV to PGND decoupling loop is the smallest and make sure the routing trace is wide enough to lower impedance.
- As the input of VCC LDO, connect a 1-µF, 25-V rated ceramic capacitor to AGND for the bypassing of the AVIN pin. TI recommends the 25-V rating, but can be lowered to 16-V rating for an application with tightly regulated 12-V input bus.
- Connect a 2.2-µF, 6.3-V (or 10 V) rated ceramic capacitor to AGND for the bypassing of the VCC pin. Placing a 1-Ω resistor between the VCC pin and VDRV pin forms a RC filter on VCC pin, which greatly reduces the noise impact from power stage driver circuit.
- For remote sensing, the connections from FB voltage divider resistors to the remote location must be a pair of PCB traces with at least 12 mil trace width, and must implement Kelvin sensing across a high bypass capacitor of 0.1 µF or higher on the sensing location. The ground connection of the remote sensing signal must be connected to the GOSNS pin. The VOUT connection of the remote sensing signal must be connected to the VOSNS pin and the top feedback resistor R_{FB_top}. To maintain stable output voltage and minimize the ripple, the pair of remote sensing lines must stay away from any noise sources such as inductor and SW node, or high frequency clock lines. TI recommends to shield the pair of remote sensing lines with ground planes above and below.
- For single-end sensing, connect the FB voltage divider resistors to a high-frequency local bypass capacitor of 0.1 µF or higher, and short GOSNS to AGND with shortest trace.
- The AGND pin 32 must be connected to a solid PGND plane. TI recommends to place AGND via close to pin 32 to route AGND from top layer to bottom layer, and then connect the AGND trace to the PGND vias (underneath IC) through either a net-tie or a 0-Ω resistor on the bottom layer.
- Connecting a resistor from pin 1 (ILIM) to AGND sets the OCL threshold. Connecting a resistor from pin 29 (SS) to AGND sets soft-start time, internal compensation, and fault response. Connecting a resistor from pin 36 (MODE) to AGND sets the switching frequency and the operation mode. TI requires not to have any capacitor on these 3 pins (ILIM, SS, and MODE). A capacitor on any of these 3 pins likely leads to a wrong detection result.
- Pin 6 (DNC) is a Do-Not-Connect pin. Pin 6 can be shorted to pin 37, which is an NC pin (No internal Connection). Do not connect pin 6 to any other net including ground.

7.4.2 Layout Example



PVIN Bypass capacitors:
1x 0402 capacitors on top layer;
2x 0805 capacitors on top layer;
2x 0805 capacitors on bottom layer

Notes for VOUT Bypass capacitors: Place ceramic capacitors on top layer; Bulk capacitors are optional and can be placed on bottom layer

Figure 7-17. Layout Recommendation

7.4.2.1 Thermal Performance on TPS548D26 Evaluation Board

The following figures are thermal results captured on the TPS548D26 evaluation board with PVIN = 12V, V_{OUT} = 1.1V conditions.

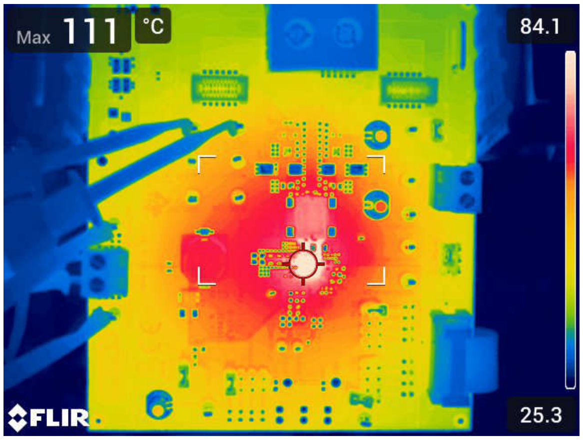


Figure 7-18. Thermal Characteristics, 600kHz FCCM, Internal LDO, 40A Load

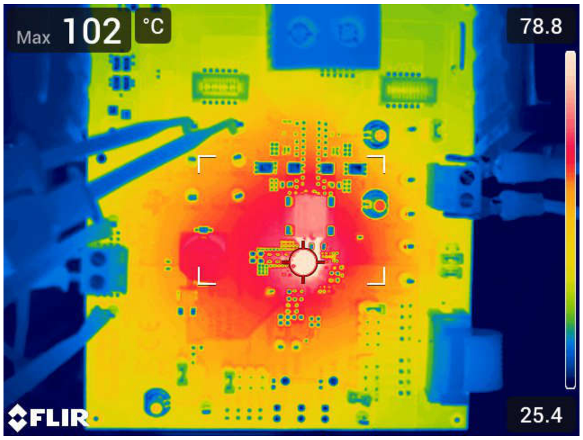


Figure 7-19. Thermal Characteristics, 600kHz FCCM, External 5V Bias, 40A Load

8 Device and Documentation Support

8.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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8.3 Trademarks

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8.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (November 2023) to Revision A (February 2024)	**Page**
• Changed document status from Advance Information to Production Data	1

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS548D26RXXR	ACTIVE	WQFN-FCRLF	RXX	37	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	548D26	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

GENERIC PACKAGE VIEW

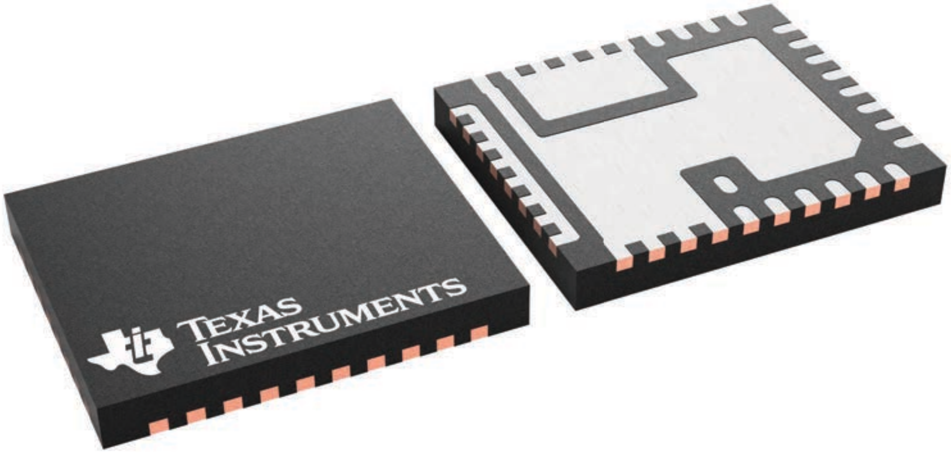
RXX 37

VQFN-FCRLF - 1.05 mm max height

5 x 6, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

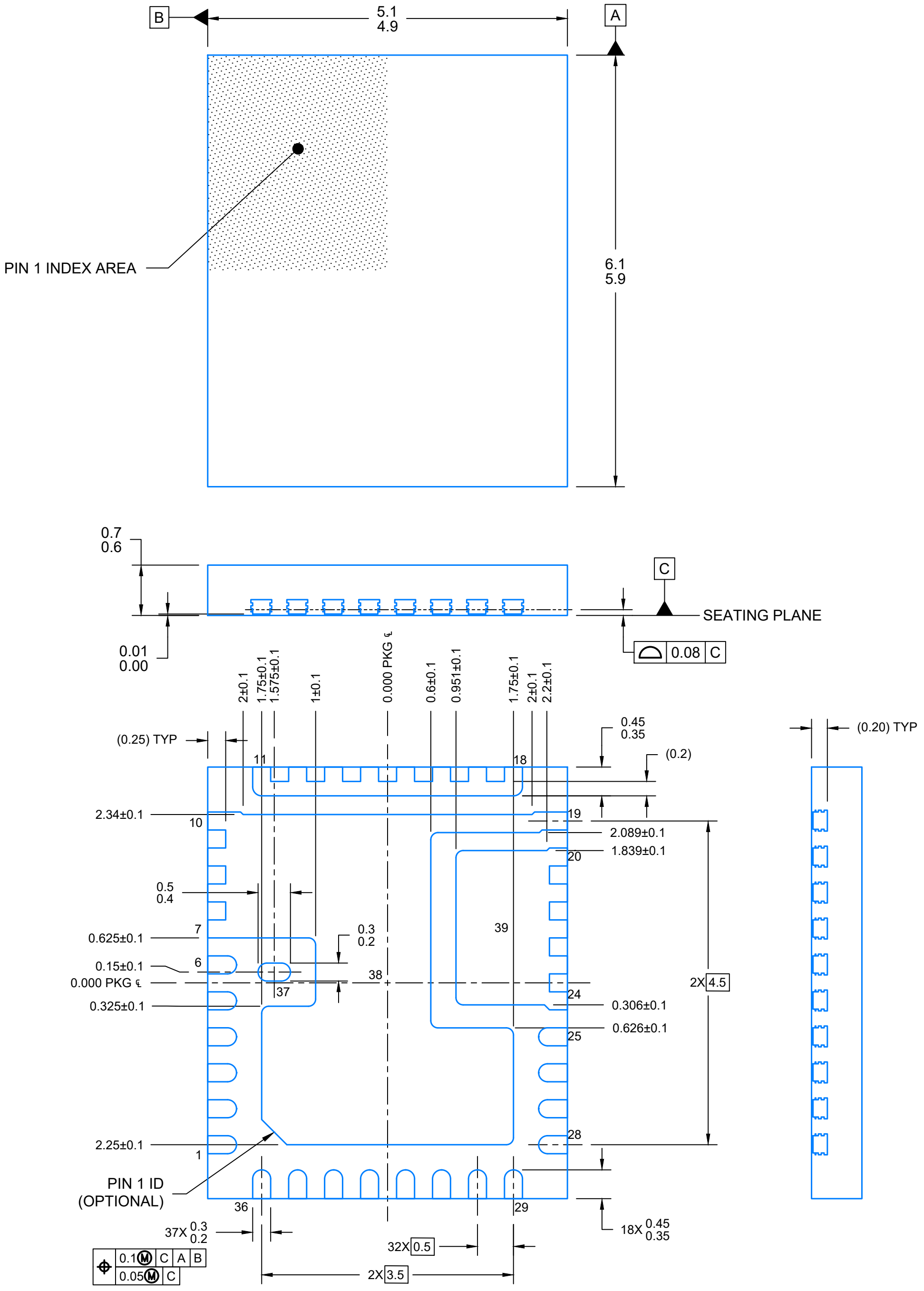


PACKAGE OUTLINE

RXX0037A

WQFN-FCRLF - 0.7 mm max height

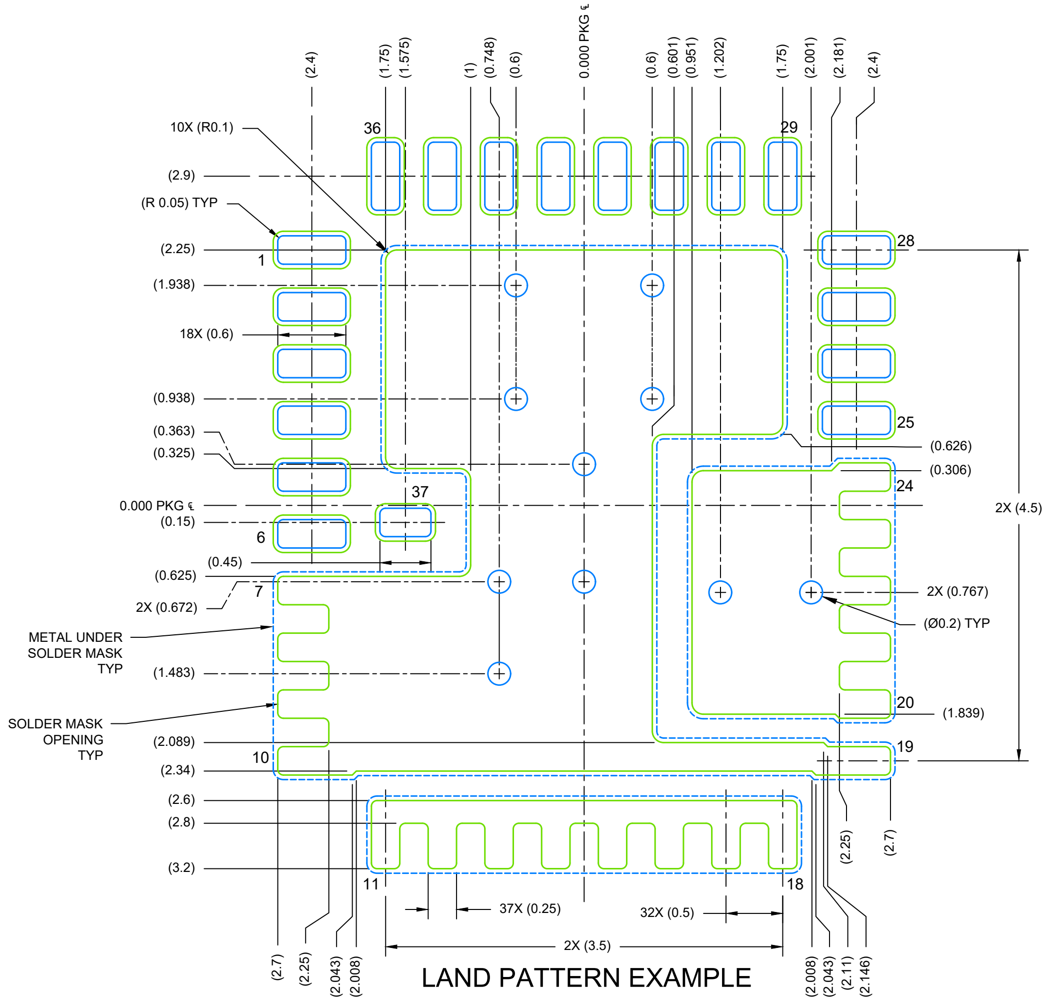
PLASTIC QUAD FLAT PACK- NO LEAD



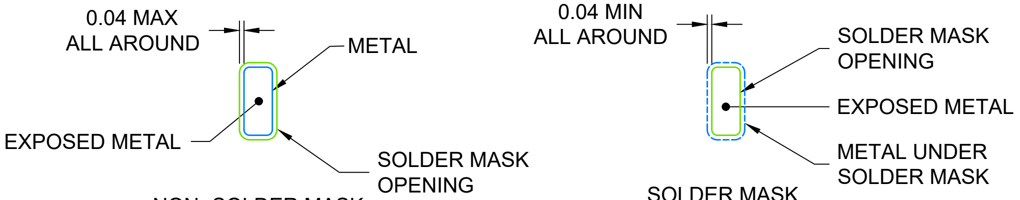
4226301/F 01/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



NON- SOLDER MASK
DEFINED
(PREFERRED)

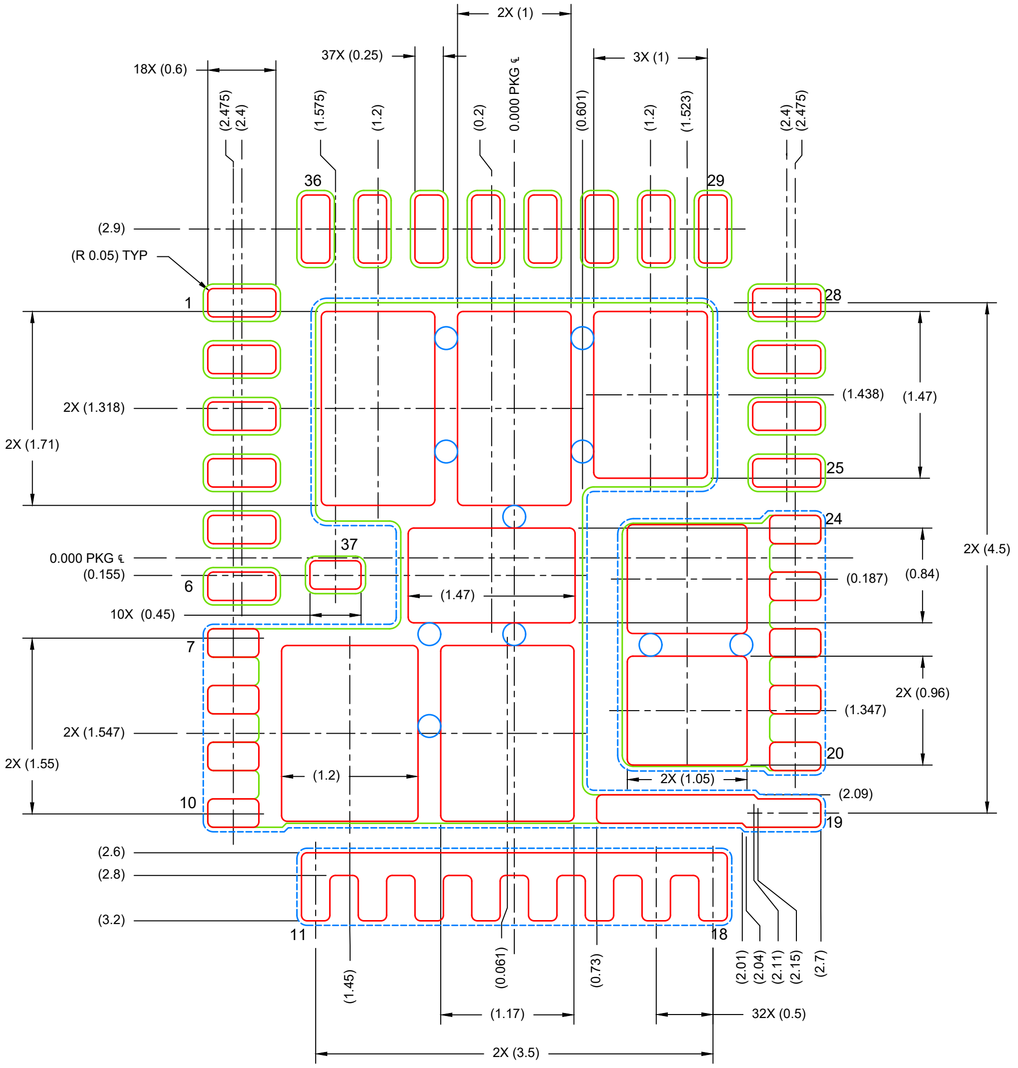
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4226301/F 01/2024

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
6. Recommended board layout is designed for 2oz copper for high current applications.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

SOLDER COVERAGE :
Thermal Pad connected to pin 7-10, 19 : 80%
Thermal Pad connected to pin 20-24 : 86%
SCALE: 15X

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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