LMV951 1-V, 2.7-MHz, Zero Crossover Rail-to-Rail Input and Output Amplifier With Shutdown

1 Features

- (Typical 1-V Supply, Unless Otherwise Noted)
- Ensured 1-V, 380-µA Single-Supply Operation
- Shutdown to 50-nA Supply Current
- Wide 2.7-MHz Bandwidth
- Rail-to-Rail Input With Zero Crossover
- No Input I_{BIAS} Current Reversal Over V_{CM} Range
- 1000-pF Output Drive Capability
- High-Output Drive Capability
  - Sink Current: 35 mA
  - Source Current: 45 mA
- Rail-to-Rail Buffered Output
  - At 600-Ω Load, 32 mV from Either Rail
  - At 2-kΩ Load, 12 mV from Either Rail
- Temperature Range −40°C to 125°C

2 Applications

- Battery Operated Systems
- Battery Monitoring
- Supply Current Monitoring

3 Description

The LMV951 amplifier is capable of operating at supply voltages from 0.9 V to 3 V with specified specs at 1-V and 1.8-V single supply.

The input common-mode range extends to both power supply rails without the offset transition zone and input bias current reversal inherent to most rail-to-rail input amplifiers.

Contrary to a conventional rail-to-rail output amplifier, the LMV951 has a buffered output stage, providing an open-loop gain which is relatively unaffected by resistive output loading. At 1-V supply voltage, the LMV951 is able to source and sink in excess of 35 mA and offers a gain bandwidth product of 2.7 MHz.

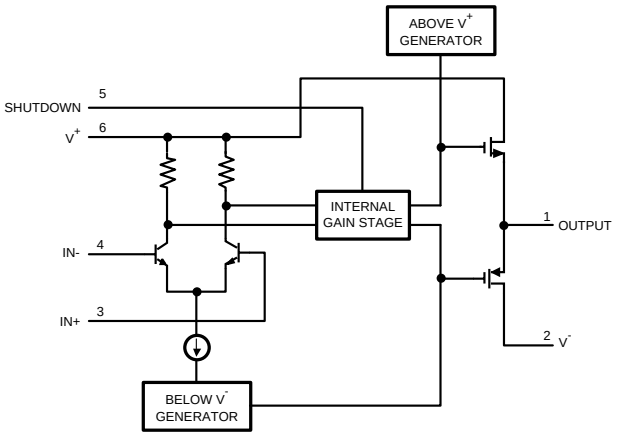
In shutdown mode, the LMV951 consumes less than 50 nA of supply current.

Device Information(1)

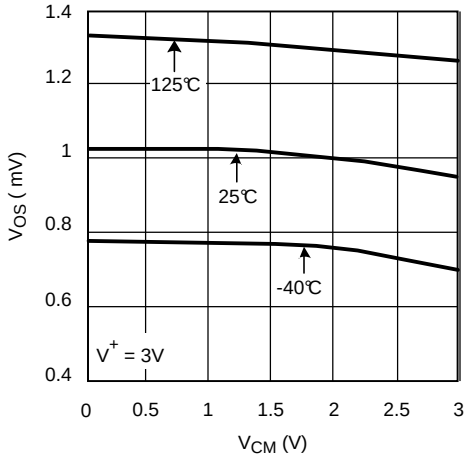
PART NUMBER	PACKAGE	BODY SIZE (NOM)
LMV951	SOT (6)	2.90 mm × 1.60 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



Offset Voltage Change vs Common Mode



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (April 2013) to Revision D **Page**

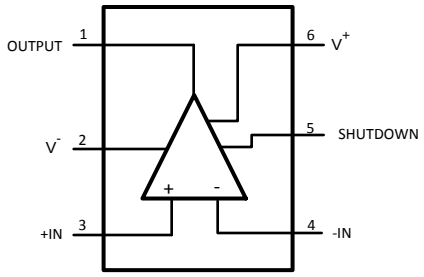
- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

Changes from Revision B (April 2013) to Revision C **Page**

- Changed layout of National Data Sheet to TI format ... 18

5 Pin Configuration and Functions

DDC Package
6-Pin SOT
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
+IN	3	I	Noninverting Input
-IN	4	I	Inverting Input
Output	1	O	Output
Shutdown	5	I	Shutdown Input
V+	6	P	Positive Supply Voltage
V-	2	P	Negative Supply Voltage

6 Specifications

6.1 Absolute Maximum Ratings

See (1)(2)

	MIN	MAX	UNIT
Supply Voltage ($V^+ – V^–$)		3.1	V
V_{IN} Differential		±0.3	V
Voltage at Input and Output Pin	(V^+) + 0.3	($V^–$) − 0.3	V
Current at Input Pin		±10	mA
Junction Temperature (3)	–40	150	°C
Mounting Temperature, Infrared or Convection (20 s)		235	°C
Storage temperature	–60	150	°C

(1) *Absolute Maximum Ratings* indicate limits beyond which damage to the device may occur. *Recommended Operating Conditions* indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and the test conditions, see the *Electrical Characteristics*.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(3) The maximum power dissipation is a function of $T_{J(MAX)}$, $R_{\theta JA}$. The maximum allowable power dissipation at any ambient temperature is $P_D = T_{J(MAX)} - T_A)/R_{\theta JA}$. All numbers apply for packages soldered directly onto a PC Board.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)(2)	±2000	V
		Machine model	±200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) Human Body Model, applicable std. MIL-STD-883, Method 3015.7. Machine Model, applicable std. JESD22-A115-A (ESD MM std. of JEDEC) Field-Induced Charge-Device Model, applicable std. JESD22-C101-C (ESD FICDM std. of JEDEC).

6.3 Recommended Operating Conditions

	MIN	MAX	UNIT
Temperature Range (1)	–40	125	°C
Supply Voltage	0.9	3	V

(1) The maximum power dissipation is a function of $T_{J(MAX)}$, $R_{\theta JA}$. The maximum allowable power dissipation at any ambient temperature is $P_D = T_{J(MAX)} - T_A)/R_{\theta JA}$. All numbers apply for packages soldered directly onto a PC Board.

6.4 Thermal Information

THERMAL METRIC (1)		LMV951 DDC (SOT) 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance (2)	170	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.
(2) The maximum power dissipation is a function of $T_{J(MAX)}$, $R_{\theta JA}$. The maximum allowable power dissipation at any ambient temperature is $P_D = T_{J(MAX)} - T_A)/R_{\theta JA}$. All numbers apply for packages soldered directly onto a PC Board.

6.5 Electrical Characteristics: 1 V

Unless otherwise specified, all limits specified for at T_A = 25°C, V^+ = 1, V^- = 0 V, V_{CM} = 0.5 V, Shutdown = 0 V, and R_L = 1 MΩ. (1)

PARAMETER		TEST CONDITIONS		MIN (2)	TYP (3)	MAX (2)	UNIT
V_{OS}	Input Offset Voltage	T_A = 25°C			1.5	2.8	mV
		At the temperature extremes				3	
TC V_{OS}	Input Offset Average Drift				0.15		µV/°C
I_B	Input Bias Current	T_A = 25°C			32	80	nA
		At the temperature extremes				85	
I_{OS}	Input Offset Current				0.2		nA
CMRR	Common-Mode Rejection Ratio	0 V ≤ V_{CM} ≤ 1 V	T_A = 25°C	67	77		dB
			At the temperature extremes	55			
		0.1 V ≤ V_{CM} ≤ 1 V	T_A = 25°C	76	85		
			At the temperature extremes	73			
PSRR	Power Supply Rejection Ratio	1 V ≤ V^+ ≤ 1.8 V, V_{CM} = 0.5 V	T_A = 25°C	70	92		dB
			At the temperature extremes	67			
		1 V ≤ V^+ ≤ 3 V, V_{CM} = 0.5 V	T_A = 25°C	68	85		
			At the temperature extremes	65			
V_{CM}	Input Common-Mode Voltage Range	CMRR ≥ 67 dB		0		1.2	V
		CMRR ≥ 55 dB	At the temperature extremes	0		1.2	
A_V	Large Signal Voltage Gain	V_{OUT} = 0.1 V to 0.9 V R_L = 600 Ω to 0.5 V	T_A = 25°C	90	106		dB
			At the temperature extremes	85			
		V_{OUT} = 0.1 V to 0.9 V R_L = 2 kΩ to 0.5 V	T_A = 25°C	90	112		
			At the temperature extremes	86			
V_{OUT}	Output Voltage Swing High	R_L = 600 Ω to 0.5 V	T_A = 25°C	50	25		mV from rail
			At the temperature extremes	62			
		R_L = 2 kΩ to 0.5 V	T_A = 25°C	25	12		
			At the temperature extremes	36			
	Output Voltage Swing Low	R_L = 600 Ω to 0.5 V	T_A = 25°C	70	32		
			At the temperature extremes	85			
		R_L = 2 kΩ to 0.5 V	T_A = 25°C	35	10		
			At the temperature extremes	40			

(1) Electrical table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions is very limited self-heating of the device.
(2) All limits are specified by testing or statistical analysis.
(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.

Electrical Characteristics: 1 V (continued)

Unless otherwise specified, all limits specified for at T_A = 25°C, V^+ = 1, V^- = 0 V, V_{CM} = 0.5 V, Shutdown = 0 V, and R_L = 1 MΩ.(1)

PARAMETER		TEST CONDITIONS		MIN(2)	TYP(3)	MAX(2)	UNIT
I_{OUT}	Output Short-Circuit Current (4)	Sourcing V_O = 0 V, $V_{IN(DIFF)}$ = ±0.2 V	T_A = 25°C	20	45		mA
			At the temperature extremes	15			
		Sinking V_O = 1 V, $V_{IN(DIFF)}$ = ±0.2 V	T_A = 25°C	20	35		
			At the temperature extremes	13			
I_S	Supply Current	Active Mode V_{SD} <0.4 V			370	480	µA
						520	
		Shutdown Mode V_{SD} >0.6 V	T_A = 25°C		0.01	1	
			At the temperature extremes			3	
SR	Slew Rate	See (5)			1.4		V/µs
GBWP	Gain Bandwidth Product				2.7		MHz
e_n	Input-Referred Voltage Noise	f = 1 kHz			25		nV/√Hz
i_n	Input-Referred Current Noise	f = 1 kHz			0.2		pA/√Hz
THD	Total Harmonic Distortion	f = 1 kHz, A_V = 1, R_L = 1 kΩ			0.02%		
I_{SD}	Shutdown Pin Current	Active Mode, V_{SD} = 0 V			.001	1	µA
		Shutdown Mode, V_{SD} = 1 V			.001	1	
V_{SD}	Shutdown Pin Voltage Range	Active Mode		0		0.4	V
		Shutdown Mode		0.65		1	

(4) The short-circuit test is a momentary test, the short-circuit duration is 1.5 ms.
(5) Number specified is the average of the positive and negative slew rates.

6.6 Electrical Characteristics: 1.8 V

Unless otherwise specified, all limits specified for at T_A = 25°C, V^+ = 1.8 V, V^- = 0 V, V_{CM} = 0.9 V, Shutdown = 0 V, and R_L = 1 MΩ.(1)

PARAMETER		TEST CONDITIONS		MIN(2)	TYP(3)	MAX(2)	UNIT
V_{OS}	Input Offset Voltage	T_A = 25°C			1.5	2.8	mV
		At the temperature extremes				3	
TC V_{OS}	Input Offset Average Drift				0.15		µV/°C
I_B	Input Bias Current	T_A = 25°C			36	80	nA
		At the temperature extremes				85	
I_{OS}	Input Offset Current				0.2		nA
CMRR	Common-Mode Rejection Ratio	0 V ≤ V_{CM} ≤ 1.8 V	T_A = 25°C	82	93		dB
			At the temperature extremes	80			
PSRR	Power Supply Rejection Ratio	1 V ≤ V^+ ≤ 1.8V, V_{CM} = 0.5 V	T_A = 25°C	70	92		dB
			At the temperature extremes	67			
		1 V ≤ V^+ ≤ 3 V, V_{CM} = 0.5 V	T_A = 25°C	68	85		
			At the temperature extremes	65			
V_{CM}	Input Common-Mode Voltage Range	CMRR ≥ 82 dB		–0.2		2	V
		CMRR ≥ 80 dB	At the temperature extremes	–0.2		2	
A_V	Large Signal Voltage Gain	V_{OUT} = 0.2 to 1.6 V R_L = 600 Ω to 0.9 V	T_A = 25°C	86	110		dB
			At the temperature extremes	83			
		V_{OUT} = 0.2 to 1.6 V R_L = 2 kΩ to 0.9 V	T_A = 25°C	86	116		
			At the temperature extremes	83			

(1) Electrical table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions is very limited self-heating of the device.
(2) All limits are specified by testing or statistical analysis.
(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.

Electrical Characteristics: 1.8 V (continued)

Unless otherwise specified, all limits specified for at T_A = 25°C, V^+ = 1.8 V, V^- = 0 V, V_{CM} = 0.9 V, Shutdown = 0 V, and R_L = 1 MΩ.(1)

PARAMETER		TEST CONDITIONS		MIN(2)	TYP(3)	MAX(2)	UNIT
V_{OUT}	Output Voltage Swing High	R_L = 600 Ω to 0.9 V	T_A = 25°C	50	33		mV from rail
			At the temperature extremes	60			
		R_L = 2 kΩ to 0.9 V	T_A = 25°C	25	13		
			At the temperature extremes	34			
	Output Voltage Swing Low	R_L = 600 Ω to 0.9 V	T_A = 25°C	80	54		
			At the temperature extremes	105			
		R_L = 2 kΩ to 0.9 V	T_A = 25°C	35	17		
			At the temperature extremes	44			
I_{OUT}	Output Short-Circuit Current (4)	Sourcing V_O = 0 V, $V_{IN(DIFF)}$ = ±0.2 V	T_A = 25°C	50	85		mA
			At the temperature extremes	35			
		Sinking V_O = 1.8 V, $V_{IN(DIFF)}$ = ±0.2 V	T_A = 25°C	45	80		
			At the temperature extremes	25			
I_S	Supply Current	Active Mode V_{SD} <0.5 V	T_A = 25°C		570	780	µA
			At the temperature extremes			880	
		Shutdown Mode V_{SD} >1.3 V	T_A = 25°C		0.3	2.2	
			At the temperature extremes			10	
SR	Slew Rate	See (5)			1.4		V/µs
GBWP	Gain Bandwidth Product				2.8		MHz
e_n	Input-Referred Voltage Noise	f = 1 kHz			25		nV/√Hz
i_n	Input-Referred Current Noise	f = 1 kHz			0.2		pA/√Hz
THD	Total Harmonic Distortion	f = 1 kHz, A_V = 1, R_L = 1 kΩ			0.02%		
I_{SD}	Shutdown Pin Current	Active Mode, V_{SD} = 0 V			.001	1	µA
		Shutdown Mode, V_{SD} = 1.8 V			.001	1	
V_{SD}	Shutdown Pin Voltage Range	Active Mode		0		0.5	V
		Shutdown Mode		1.45		1.8	

(4) The short-circuit test is a momentary test, the short-circuit duration is 1.5 ms.
(5) Number specified is the average of the positive and negative slew rates.

6.7 Typical Characteristics

Unless otherwise specified, all limits are specified for T_A = 25°C, V^+ = 1 V, V^- = 0 V, V_{CM} = V^+/2 = V_O.

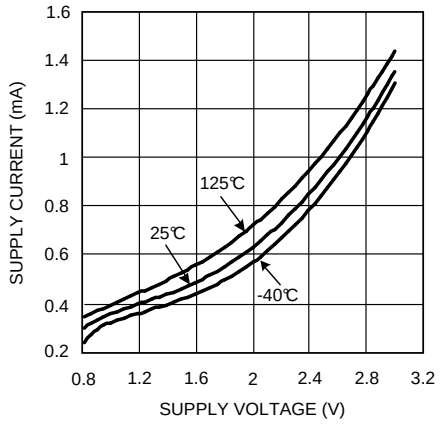


Figure 1. Supply Current vs Supply Voltage

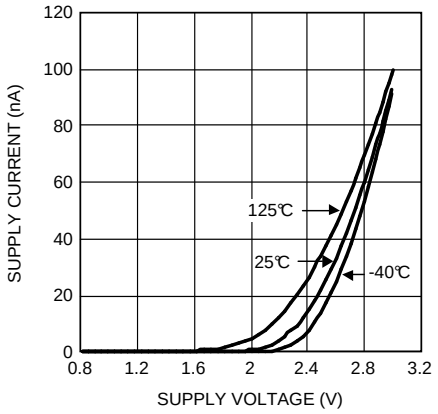


Figure 2. Supply Current vs Supply Voltage in Shutdown Mode

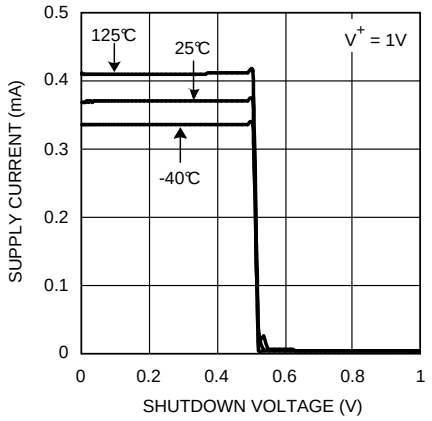


Figure 3. Supply Current vs Shutdown Voltage

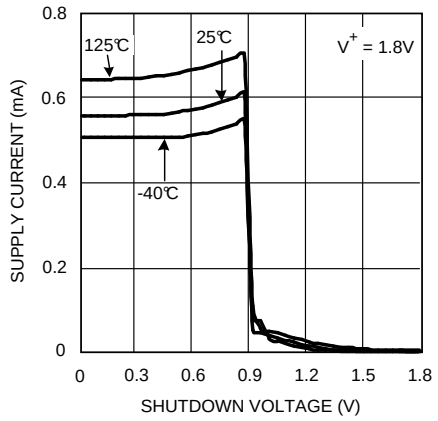


Figure 4. Supply Current vs Shutdown Voltage

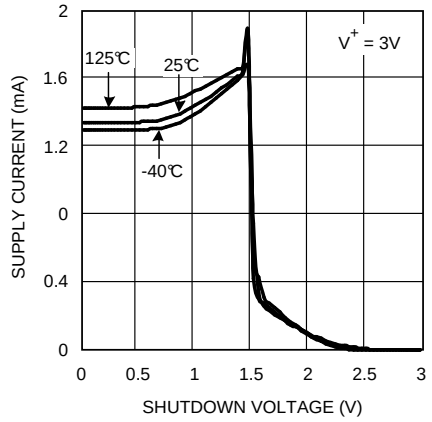


Figure 5. Supply Current vs Shutdown Voltage

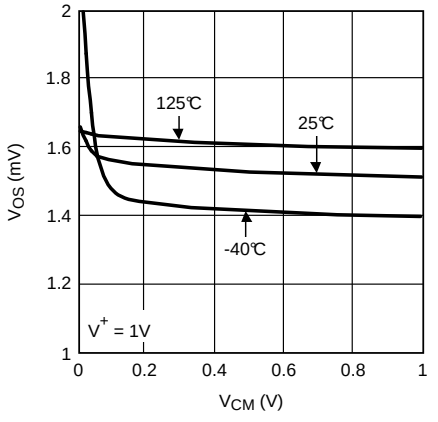


Figure 6. V_{OS} vs V_{CM}

Typical Characteristics (continued)

Unless otherwise specified, all limits are specified for T_A = 25°C, V^+ = 1 V, V^- = 0 V, V_{CM} = V^+/2 = V_O.

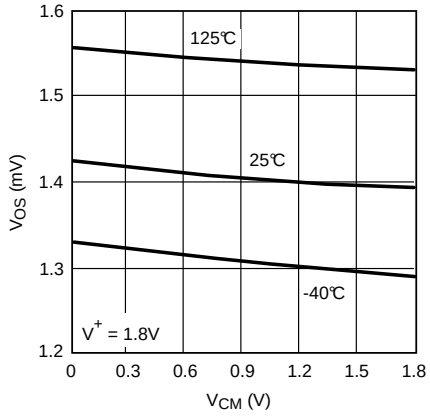


Figure 7. V_{OS} vs V_{CM}

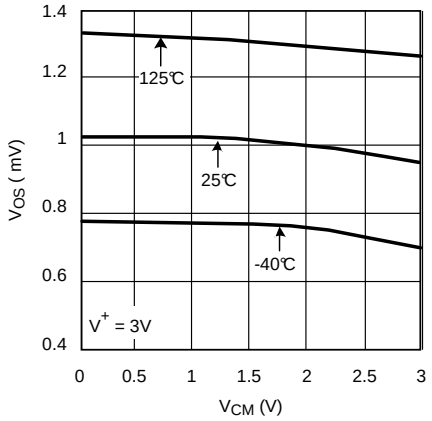


Figure 8. V_{OS} vs V_{CM}

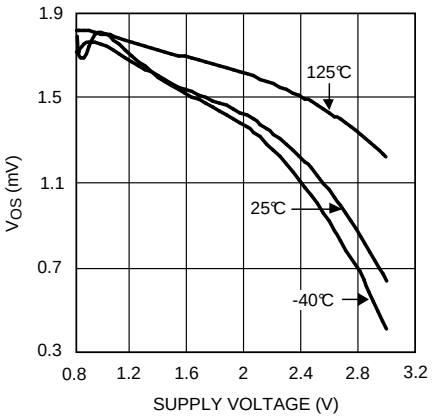


Figure 9. V_{OS} vs Supply Voltage

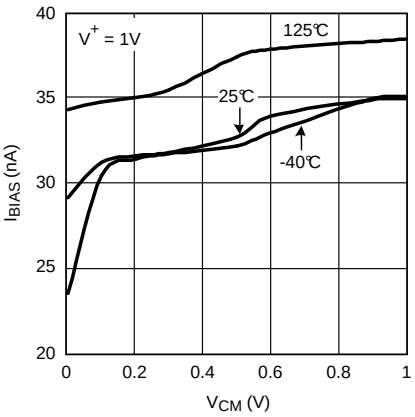


Figure 10. I_{BIAS} vs V_{CM}

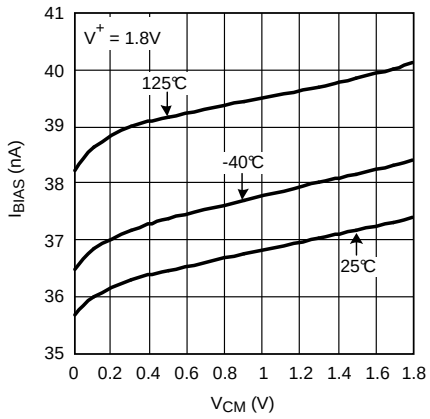


Figure 11. I_{BIAS} vs V_{CM}

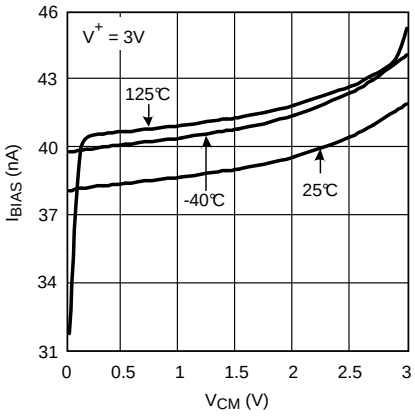


Figure 12. I_{BIAS} vs V_{CM}

Typical Characteristics (continued)

Unless otherwise specified, all limits are specified for T_A = 25°C, V^+ = 1 V, V^- = 0 V, V_{CM} = V^+/2 = V_O.

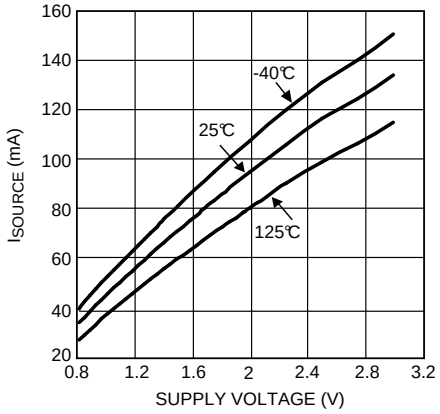


Figure 13. Sourcing Current vs Supply Voltage

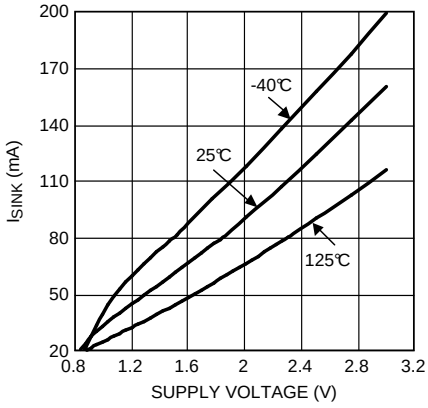


Figure 14. Sinking Current vs Supply Voltage

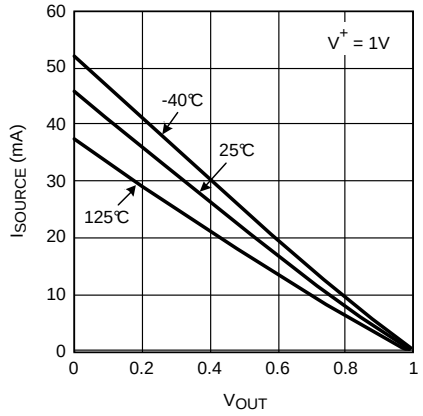


Figure 15. Sourcing Current vs Output Voltage

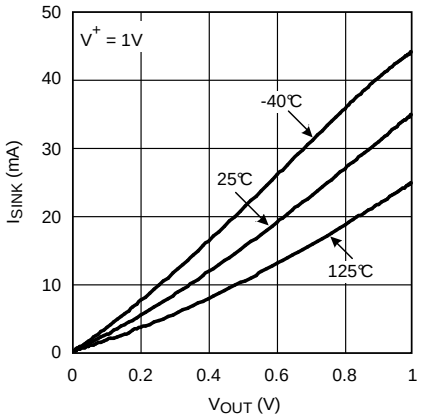


Figure 16. Sinking Current vs Output Voltage

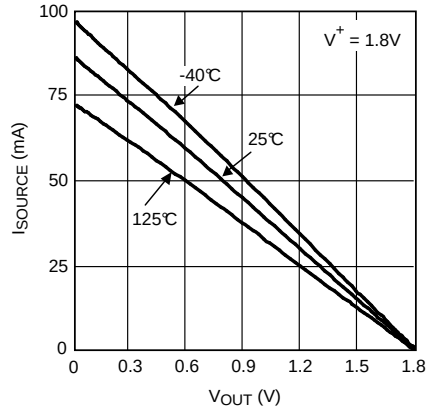


Figure 17. Sourcing Current vs Output Voltage

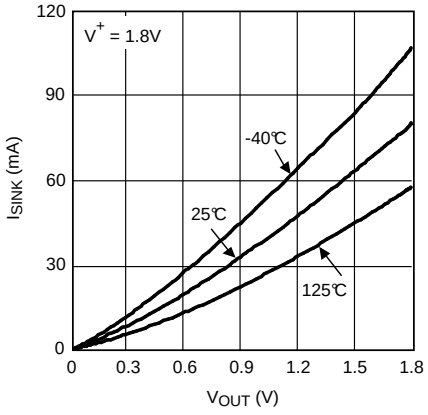


Figure 18. Sinking Current vs Output Voltage

Typical Characteristics (continued)

Unless otherwise specified, all limits are specified for T_A = 25°C, V^+ = 1 V, V^- = 0 V, V_{CM} = V^+/2 = V_O.

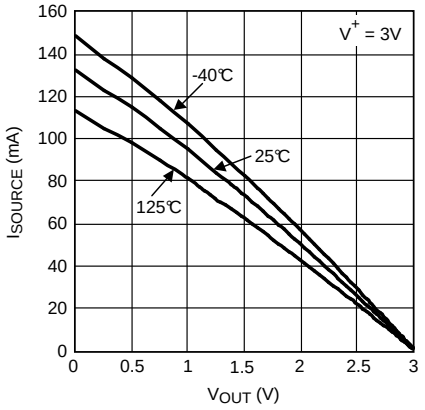


Figure 19. Sourcing Current vs Output Voltage

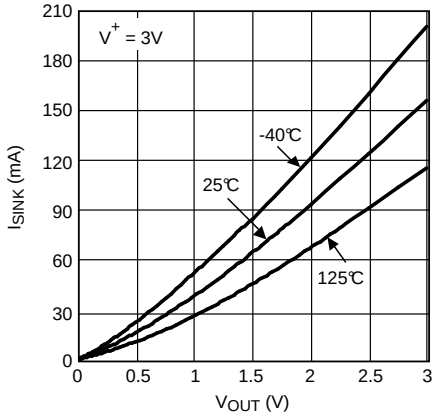


Figure 20. Sinking Current vs Output Voltage

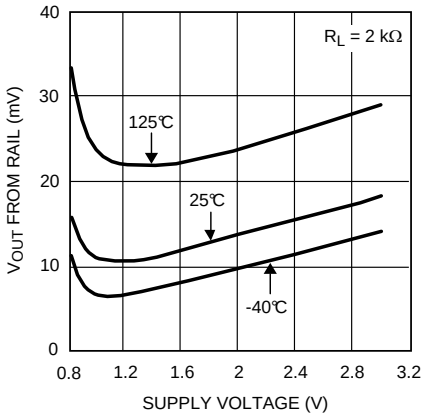


Figure 21. Positive Output Swing vs Supply Voltage

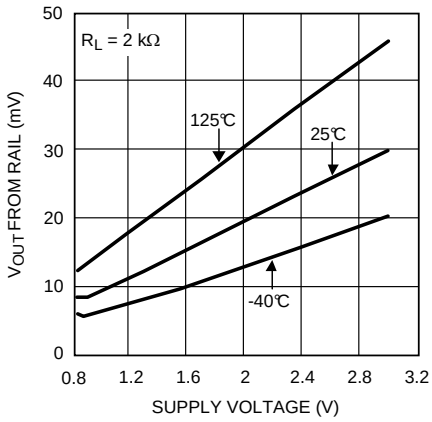


Figure 22. Negative Output Swing vs Supply Voltage

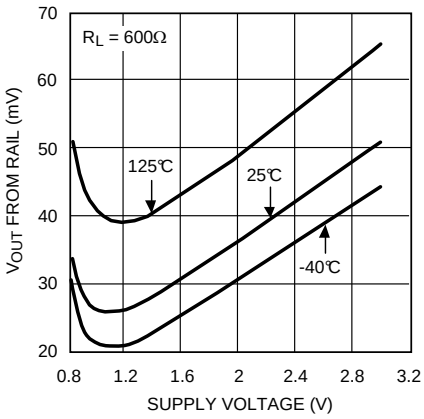


Figure 23. Positive Output Swing vs Supply Voltage

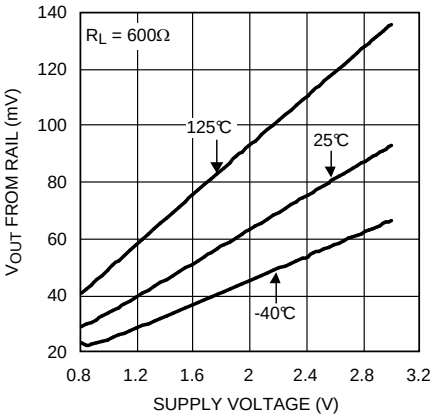


Figure 24. Negative Output Swing vs Supply Voltage

Typical Characteristics (continued)

Unless otherwise specified, all limits are specified for T_A = 25°C, V^+ = 1 V, V^- = 0 V, V_{CM} = V^+/2 = V_O.

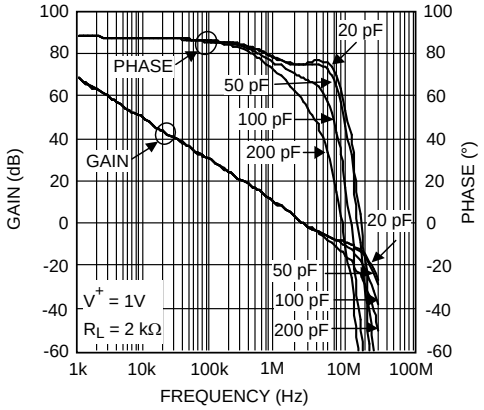


Figure 25. Open Loop Gain and Phase With Capacitive Load

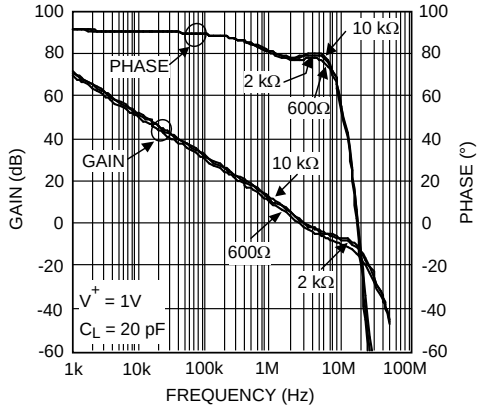


Figure 26. Open Loop Gain and Phase With Resistive Load

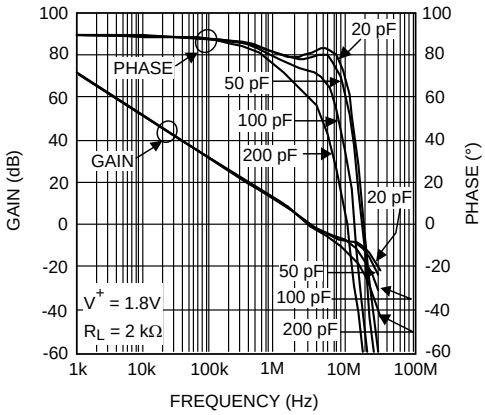


Figure 27. Open Loop Gain and Phase With Capacitive Load

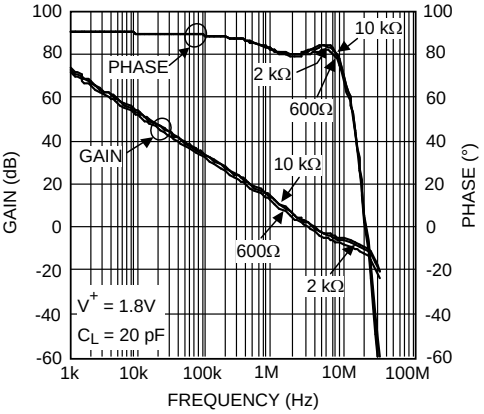


Figure 28. Open Loop Gain and Phase With Resistive Load

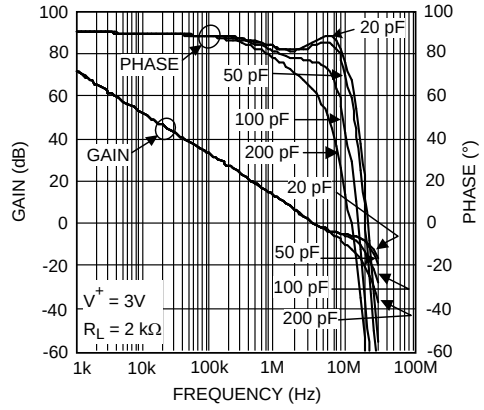


Figure 29. Open Loop Gain and Phase With Capacitive Load

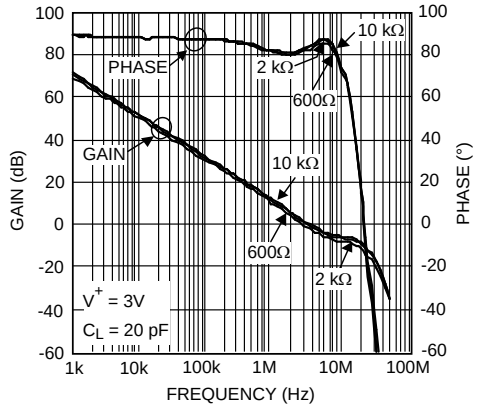


Figure 30. Open Loop Gain and Phase With Resistive Load

Typical Characteristics (continued)

Unless otherwise specified, all limits are specified for T_A = 25°C, V^+ = 1 V, V^- = 0 V, V_{CM} = V^+/2 = V_O.

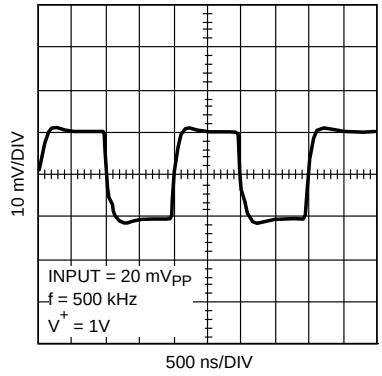


Figure 31. Small Signal Transient Response, A_V = +1

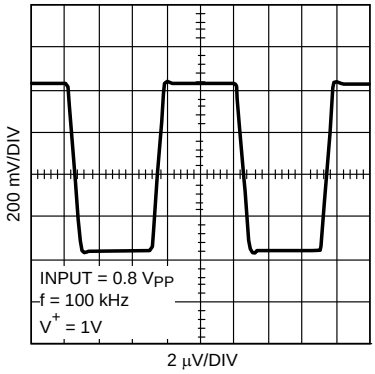


Figure 32. Large Signal Transient Response, A_V = +1

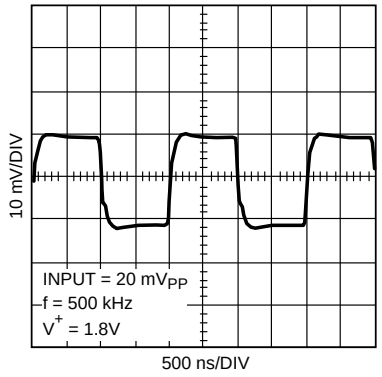


Figure 33. Small Signal Transient Response, A_V = +1

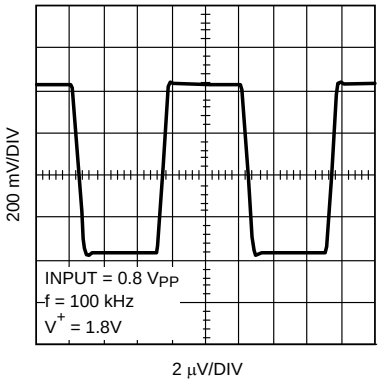


Figure 34. Large Signal Transient Response, A_V = +1

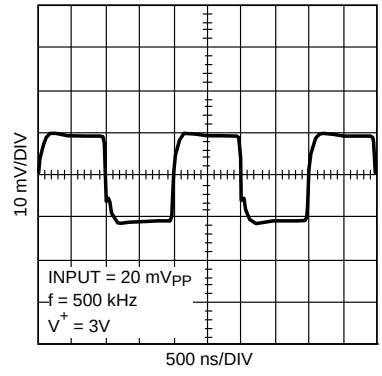


Figure 35. Small Signal Transient Response, A_V = +1

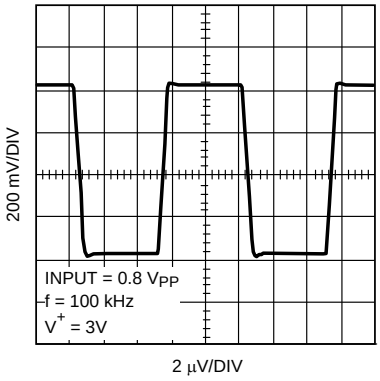


Figure 36. Large Signal Transient Response, A_V = +1

Typical Characteristics (continued)

Unless otherwise specified, all limits are specified for T_A = 25°C, V^+ = 1 V, V^- = 0 V, V_{CM} = V^+/2 = V_O.

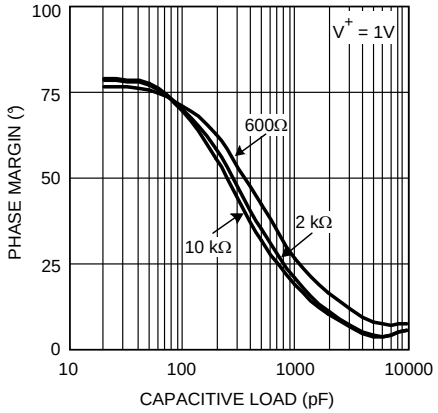


Figure 37. Phase Margin vs Capacitive Load (Stability)

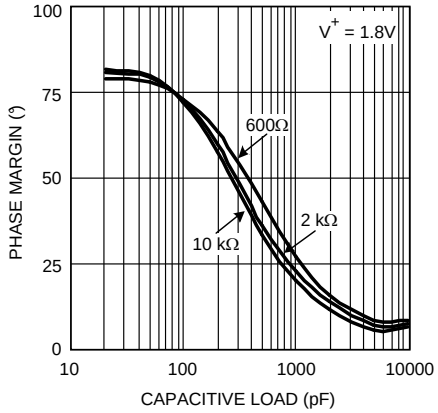


Figure 38. Phase Margin vs Capacitive Load (Stability)

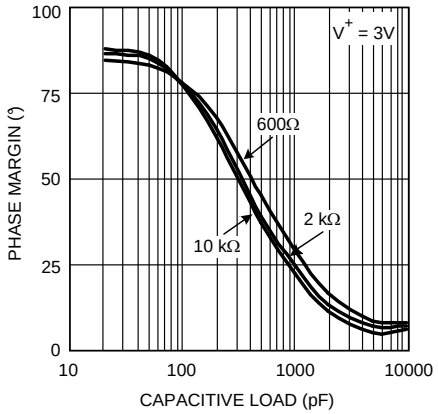


Figure 39. Phase Margin vs Capacitive Load (Stability)

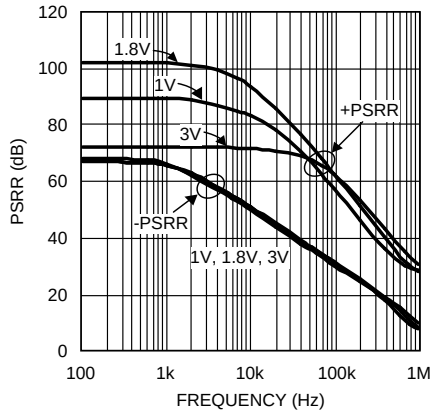


Figure 40. PSRR vs Frequency

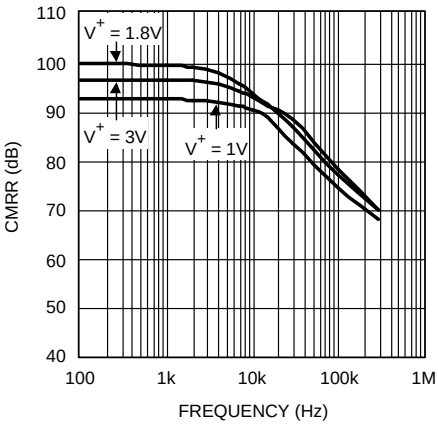


Figure 41. CMRR vs Frequency

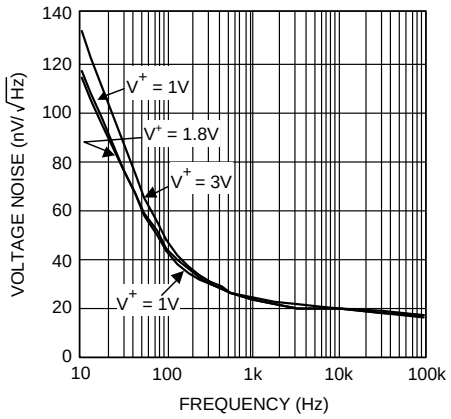


Figure 42. Input Referenced Voltage Noise vs Frequency

Typical Characteristics (continued)

Unless otherwise specified, all limits are specified for T_A = 25°C, V^+ = 1 V, V^- = 0 V, V_{CM} = V^+/2 = V_O.

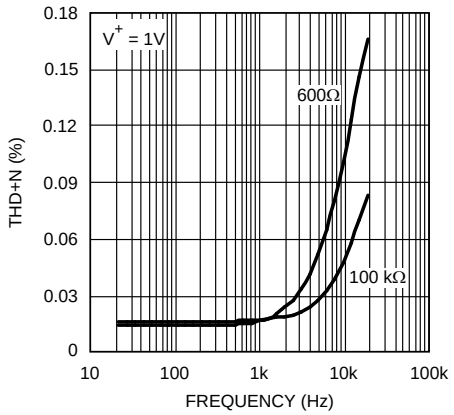


Figure 43. THD+N vs Frequency

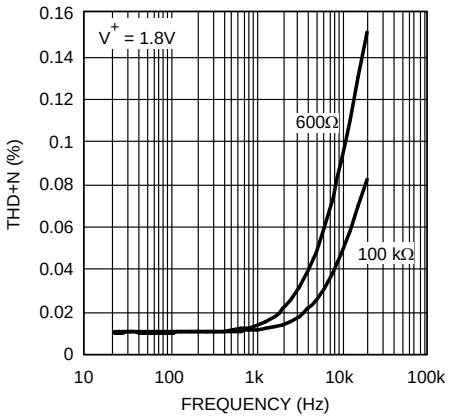


Figure 44. THD+N vs Frequency

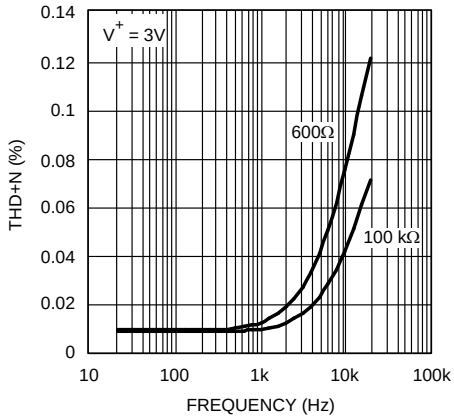


Figure 45. THD+N vs Frequency

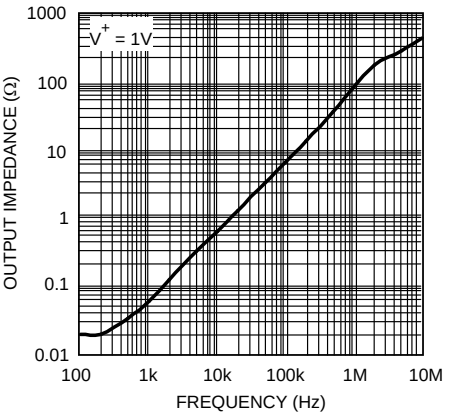


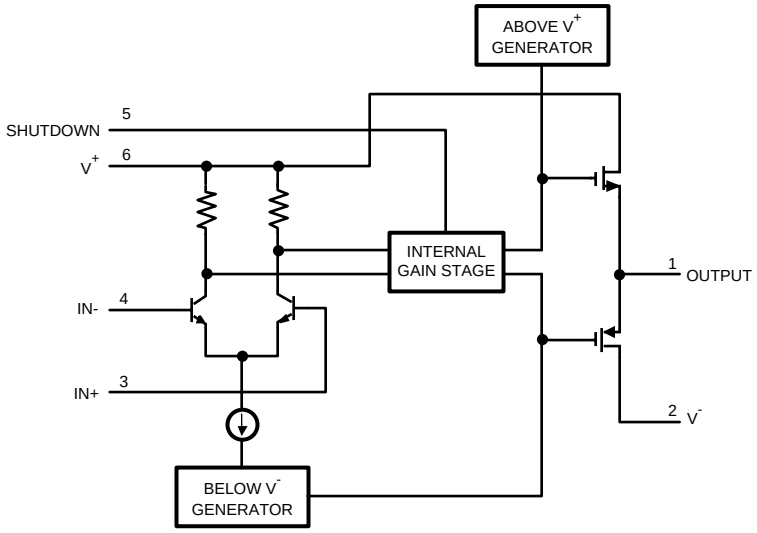
Figure 46. Closed Loop Output Impedance vs Frequency

7 Detailed Description

7.1 Overview

The LMV951 device is low-voltage operational amplifier that utilizes an internal charge pump which allows for full rail-to-rail input and output operation from 1-V to 3-V supplies. An internal switching frequency from 10 MHz to 15 MHz is used for generating the internal voltages.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Battery Operated Systems

The maximum operating voltage is 3 V and the operating characteristics are ensured down to 1 V which makes the LMV951 an excellent choice for battery operated systems using one or two NiCd or NiMH cells. The LMV951 is also functional at 0.9 V making it an appropriate choice for a single cell alkaline battery.

7.3.2 Small Size

The small footprint of the LMV951 package is ideal for high density board systems. By using the small 6-pin SOT package, the amplifier can be placed closer to the signal source, reducing noise pickup and increasing signal integrity.

7.4 Device Functional Modes

7.4.1 Shutdown Capability

While in shutdown mode, the LMV951 typically consumes less than 50 nA of supply current making it ideal for power conscious applications. Full functionality is restored within 3 µs of enable.

The output is in a high impedance state during shutdown. Voltages may be applied to the inputs and output during shutdown provided they are within the legal V+ to V- range.

7.4.2 Rail-to-Rail Input

The bipolar input stage provides rail-to-rail input operation with no input bias current reversal and a constant input offset voltage over the entire input common-mode range.

Device Functional Modes (continued)

The input contains protection diodes between the inputs to limit the differential voltage (voltage between the input pins). The LMV951 should NOT be used for comparator applications as the diodes will clamp the inputs together. These diodes may also cause issues with follower configurations during shutdown as crosstalk may occur between the input pins through these diodes.

7.4.3 Rail-to-Rail Output

The CMOS output stage provides a gain that is virtually independent of resistive loads and an output drive current in excess of 35 mA at 1 V. A further benefit of the output stage is that the LMV951 is stable in positive unity gain at capacitive loads in excess of 1000 pF.

The internal charge pumps are used to provide the needed headroom for the internal gate drive circuitry and does not enable the output to swing beyond the rails. The output swing is still bound by the V+ and V- rails.

7.4.4 Driving Capacitive Load

The unity gain follower is the most sensitive op amp configuration to capacitive loading. The LMV951 can drive up to 10,000 pF in this configuration without oscillation. If the application requires a phase margin greater than those shown in the datasheet graphs, a snubber network is recommended. The snubber offers the advantage of reducing the output signal ringing while maintaining the output swing which ensures a wider dynamic range; this is especially important at lower supply voltages.

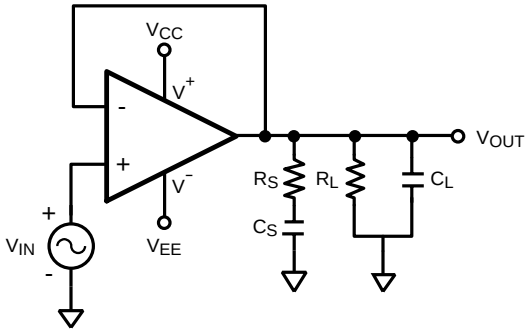


Figure 47. Snubber Network to Improve Phase Margin

Table 1 gives recommended values for some common values of large capacitors. For these values R_L = 2 kΩ.

Table 1. Recommended Values for Snubbing Network

C_L	R_S	C_S
500 pF	330Ω	6800 pF
680 pF	270Ω	8200 pF
1000 pF	220Ω	.015 µF

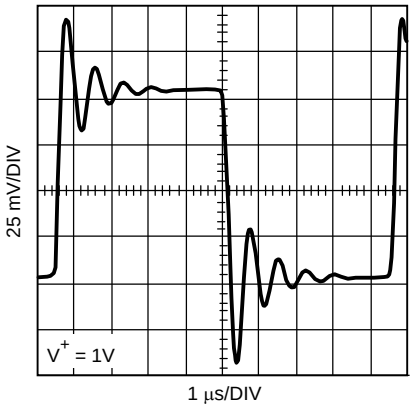


Figure 48. 1000 pF and No Snubber

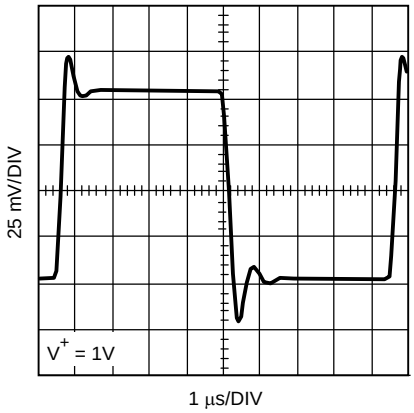


Figure 49. 1000 pF With Snubber

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The unique internal charge pumps allows the LMV951 to fully function at supply voltages as low as 0.9 V. This opens up new possibilities for unique low-voltage circuits that are not possible with standard amplifiers.

8.2 Typical Applications

8.2.1 Two Wire Line Transmission

The circuit shown in Figure 50 can drive a long cable using only two wires; a combined single signal and power wire and ground. The robust output stage and low operating voltage of the LMV951 makes it an excellent choice for driving long cables.

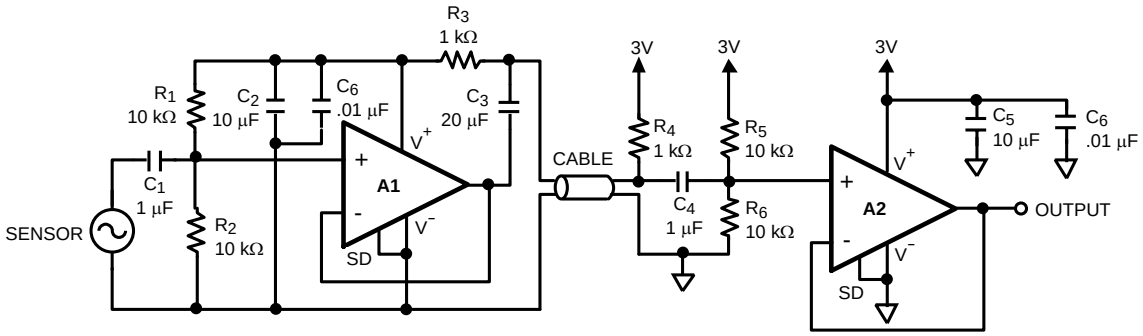


Figure 50. Two Wire Line Driver

8.2.1.1 Design Requirements

When many sensors are located remotely from the control area the wiring becomes a significant expense. Using only two wires helps minimize the wiring expense in a large project such as an industrial plant. It is desired to both provide a buffered signal from the sensor as well as provide power to the sensor amplifier.

8.2.1.2 Detailed Design Procedure

TI recommends a power supply of 3 V to power this system. A1 and A2 are set up as unity gain buffers. Configuring A1 with the required gain is simple if a gain of greater than one is required. C_1 along with R_1 and R_2 are used to ensure the correct DC operating point at the input of A1.

C_4 along with R_5 and R_6 are used to set up the correct DC operating point for A2. C_1, C_3, and C_4 have been selected to give about a 20% droop with a 1-kHz square wave input.

8.2.1.3 Application Curves

Figure 51 shows a 25-kHz signal after passing though 1000 ft of twisted-pair cable. Figure 52 shows a 200 kHz signal after passing through 50 ft of twisted-pair cable.

Typical Applications (continued)

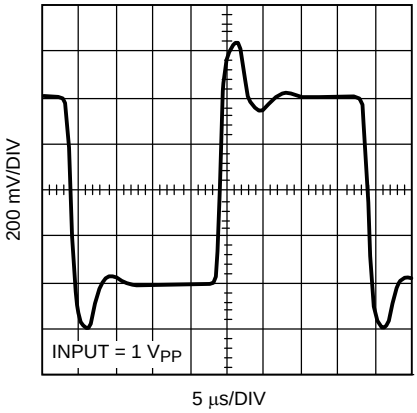


Figure 51. 25 kHz Through 1000 ft

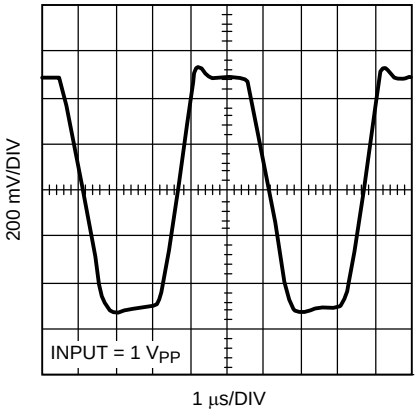


Figure 52. 200 kHz Through 50 ft

8.2.2 Bridge Configuration Amplifier

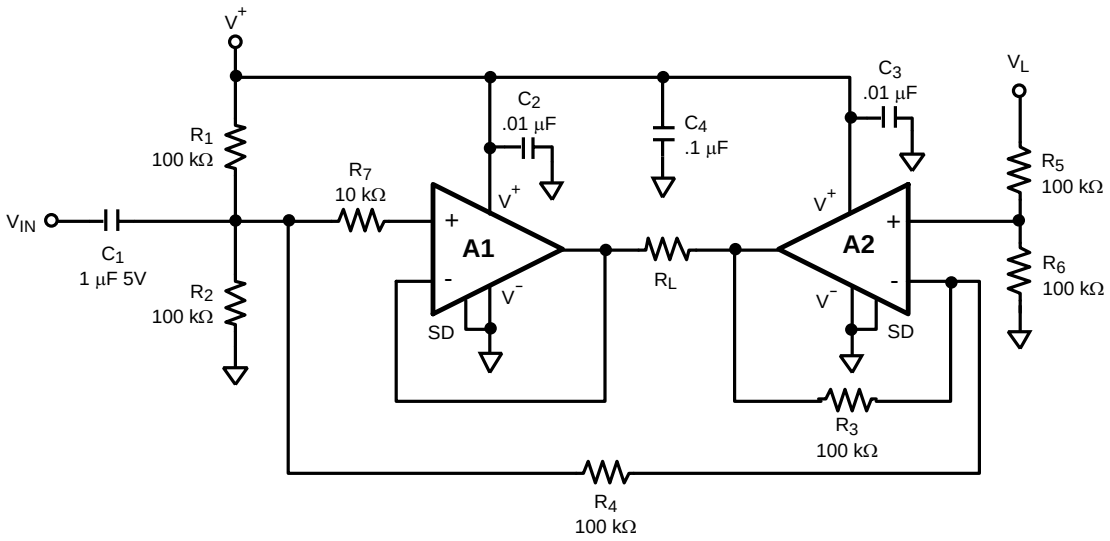


Figure 53. Bridge Amplifier

Some applications may benefit from doubling the voltage across the load. With V^+ = 1 V a bridge configuration can provide a 2-V_{PP} output to the load with a resistance as low as 300 Ω. The output stage of the LMV951 enables it to drive a load of 120 Ω and still swing at least 70% of the supply rails.

The bridge configuration shown in Figure 53 enables the amplifier to maintain a low dropout voltage thus maximizing its dynamic range. It has been configured in a gain of 1 and uses the fewest number of parts.

Resistor values have been selected to keep the current consumption to a minimum and voltage errors due to bias currents negligible. Using the selected resistor values makes this circuit quite practical in a battery operated design. R_1, R_2 and R_5, R_6 set up a virtual ground that is half of V^+. The accuracy of the resistor values will establish how well the two virtual grounds match. Any errors in the virtual grounds will show as current across R_L when there is no input signal.

Typical Applications (continued)

AC coupling the input signal sets the DC bias point of this signal to the virtual ground of the circuit. Using the large resistor values with a 1-µF capacitor (C_1) sets the frequency rolloff of this circuit below 10 Hz.

- C_2 and C_3 are .01-µF ceramic capacitors that must be located as close as possible to pin 6, the V^+ pin. As covered in the power supply bypassing section these capacitors must have low ESR and a self resonant frequency above 15 MHz.
- C_4 is a 1 µF tantalum or electrolytic capacitor that should also be located close to the supply pin.
- To use the shutdown feature tie pin 5 of the two parts together and connect through a 470-kΩ resistor to V^+. Add a switch between pin 5 and ground. Closing the switch keeps the parts in the active mode, opening the switch sets the parts in the shutdown mode without adding any additional current to V^+.

8.2.3 Virtual Ground Circuit

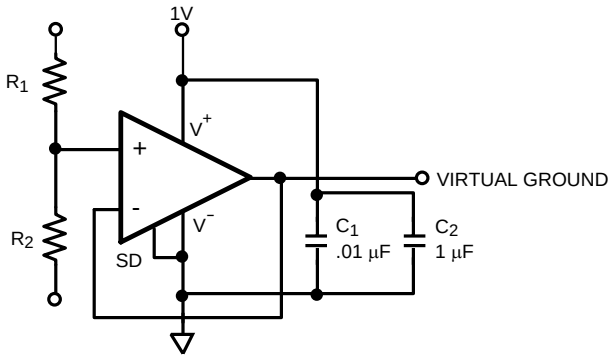


Figure 54. Virtual Ground Circuit

Figure 54 shows the LMV951 being used in a system establishing a virtual ground. Having a buffered output stage gives this part the ability to handle load currents higher than 35 mA at 1 V.

R_3 and R_4 are used to set the voltage of the virtual ground. To maintain low noise the values should be from 1 kΩ to 10 kΩ. C_1 and C_2 provide the recommended bypassing for the LMV951. These capacitors must be placed as close as possible to pins 2 and 6.

9 Power Supply Recommendations

As in any high performance IC, proper power supply bypassing is necessary for optimizing the performance of the LMV951.

The internal 15-MHz voltage generator needs proper supply bypassing for optimum operation. A surface mount ceramic .01-µF capacitor must be located as close as possible to the V^+ and V^- pins (pins 2 and 6). This capacitor needs to have low ESR and a self resonant frequency above 15 MHz. A small tantalum or electrolytic capacitor with a value from 1 µF to 10 µF must also be located close to the LMV951.

10 Layout

10.1 Layout Guidelines

- The V+ pin must be bypassed to ground with a low-ESR capacitor. The optimum placement is closest to the V+ and ground pins.
- Take care to minimize the loop area formed by the bypass capacitor connection between V+ and ground.
- The ground pin should be connected to the PCB ground plane at the pin of the device.
- The feedback components should be placed as close to the device as possible minimizing strays.

10.2 Layout Example

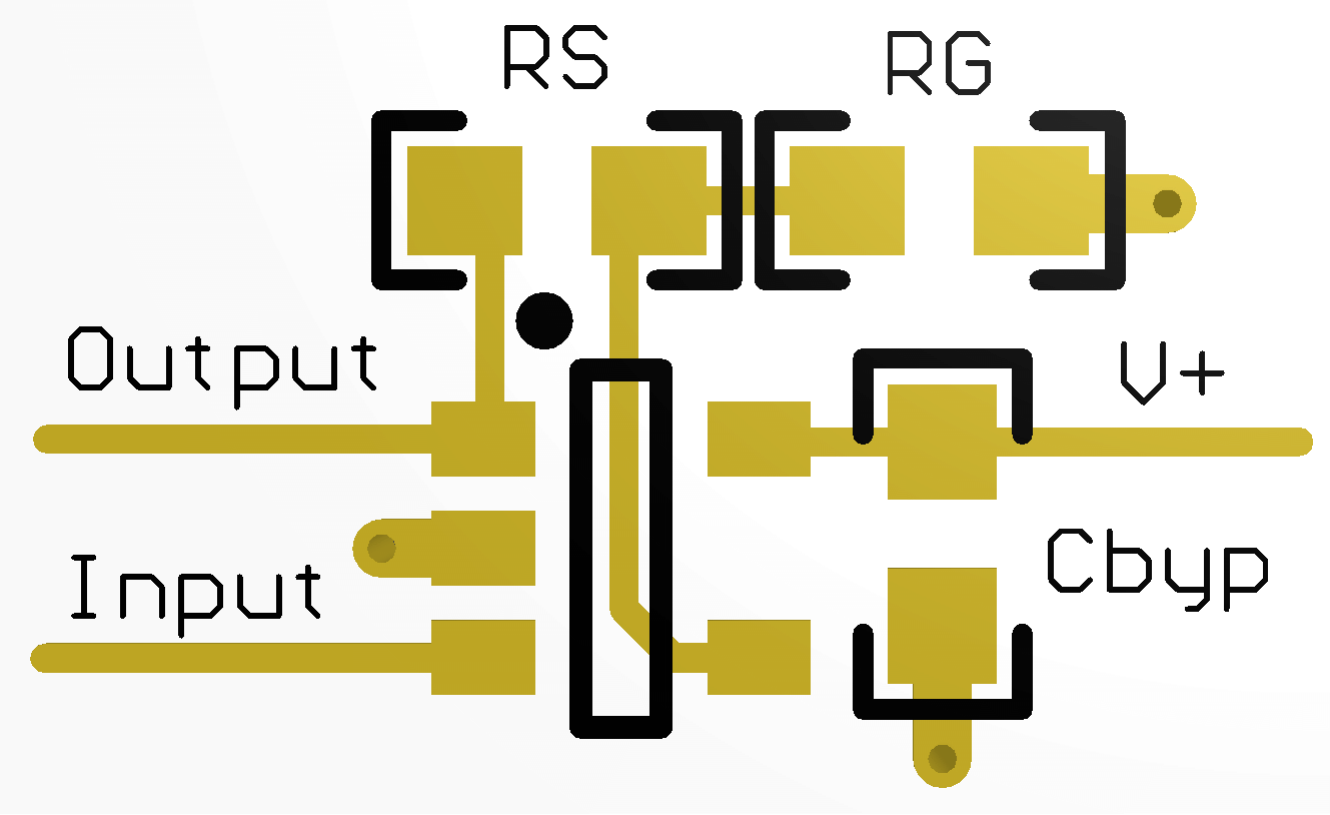


Figure 55. Layout Recommendation

11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

LMV951 PSPICE Model, http://www.ti.com/lit/zip/snom029

TINA-TI SPICE-Based Analog Simulation Program, http://www.ti.com/tool/tina-ti

DIP Adapter Evaluation Module, http://www.ti.com/tool/dip-adapter-evm

TI Universal Operational Amplifier Evaluation Module, http://www.ti.com/tool/opampevm

TI Filterpro Software, http://www.ti.com/tool/filterpro

WEBENCH® Amplifier Designer, http://www.ti.com/lsds/ti/analog/webench/amplifiers.page

11.2 Documentation Support

11.2.1 Related Documentation

For additional applications, see the following: *AN-31 Op Amp Circuit Collection*, SNLA140

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

E2E is a trademark of Texas Instruments.
WEBENCH is a registered trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMV951MK/NOPB	ACTIVE	SOT-23-THIN	DDC	6	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	AS3A	Samples
LMV951MKX/NOPB	ACTIVE	SOT-23-THIN	DDC	6	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	AS3A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

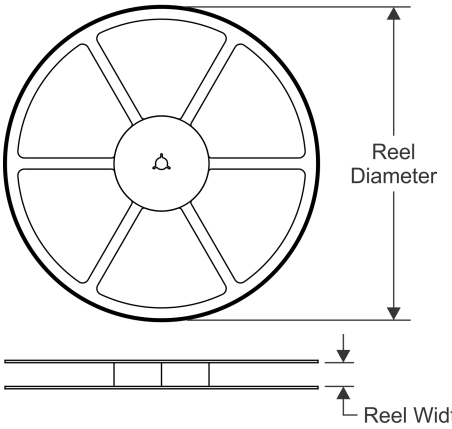
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

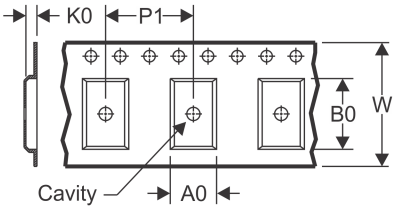
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

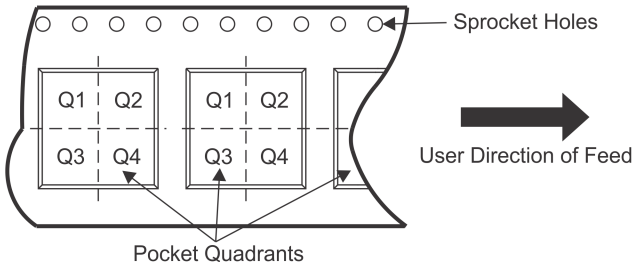


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

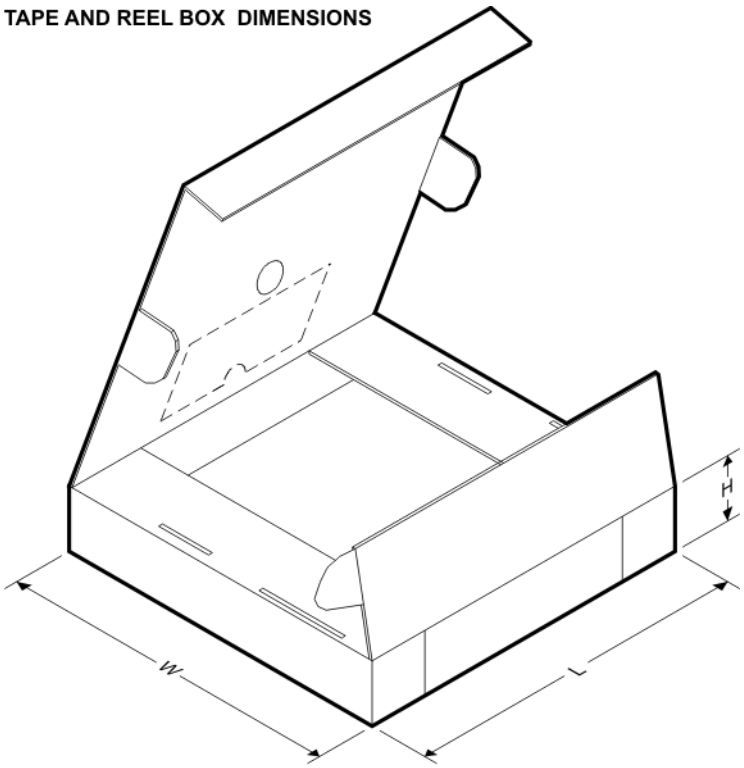
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMV951MK/NOPB	SOT-23-THIN	DDC	6	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV951MKX/NOPB	SOT-23-THIN	DDC	6	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

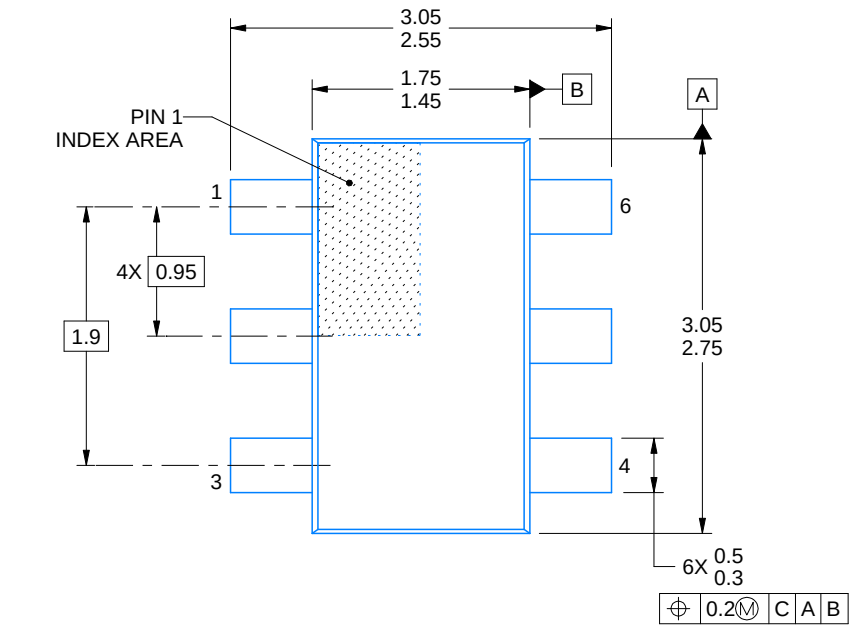
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMV951MK/NOPB	SOT-23-THIN	DDC	6	1000	208.0	191.0	35.0
LMV951MKX/NOPB	SOT-23-THIN	DDC	6	3000	208.0	191.0	35.0

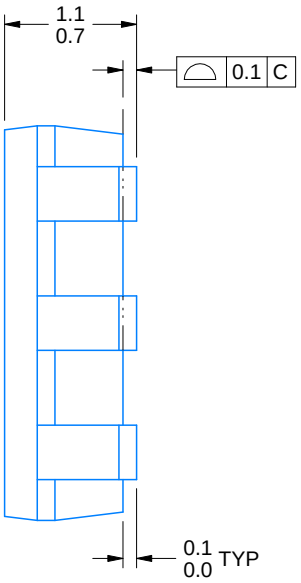
PACKAGE OUTLINE

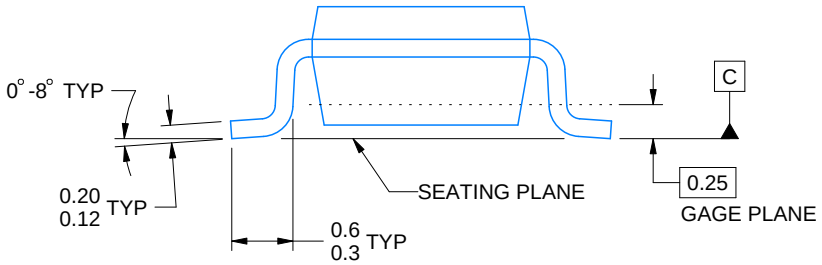
DDC0006A

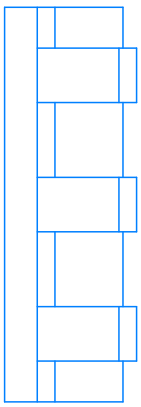
SOT-23 - 1.1 max height

SMALL OUTLINE TRANSISTOR









ALTERNATIVE PACKAGE
SINGULATION VIEW

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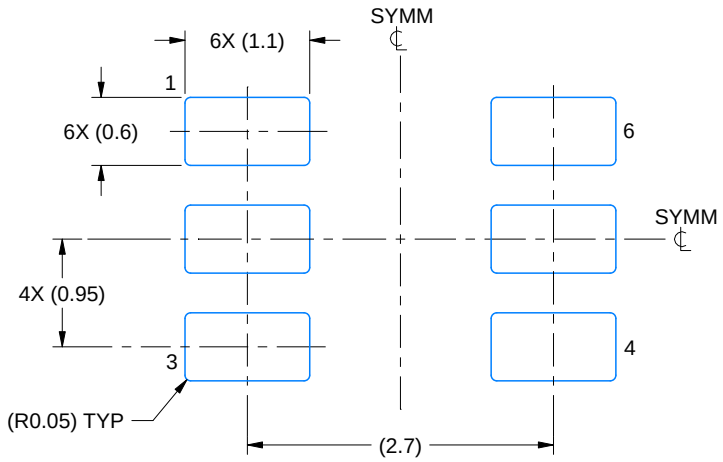
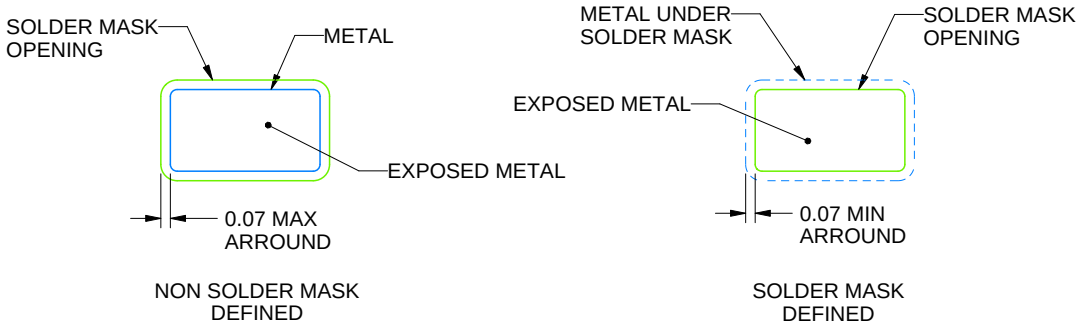
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-193.



LAND PATTERN EXAMPLE
EXPLOSED METAL SHOWN
SCALE:15X



SOLDERMASK DETAILS

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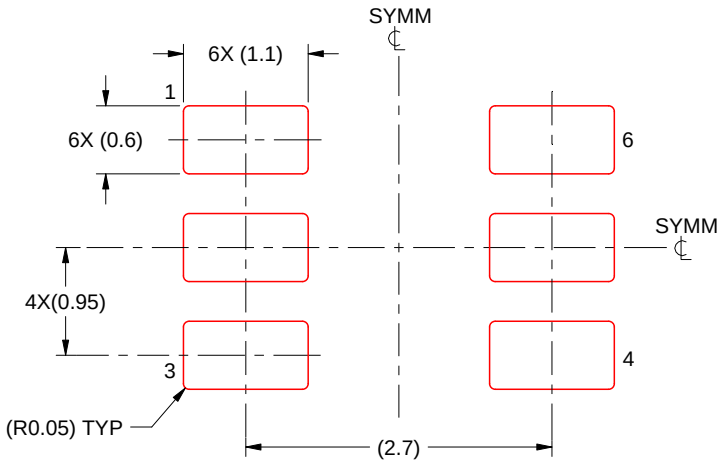
NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:15X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

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