TEXAS INSTRUMENTS
TPS6286A06, TPS6286B10
SLUSFG2 – SEPTEMBER 2024

TPS6286Axx and TPS6286Bxx 2.4V to 5.5V Input, 6A, 8A, and 10A Synchronous Step-Down Converter in 2mm × 3mm QFN Package With FB/I²C Interface

ADVANCE INFORMATION

1 Features

- DCS-Control topology for fast transient response
- 8mΩ and 8mΩ internal power MOSFETs
- 0.7% output voltage accuracy
- 5.1µA operating quiescent current
- 2.4V to 5.5V input voltage range
- 1.2MHz switching frequency
- FB version (TPS6286Axx) output voltage:
  - Adjustable from 0.6V to Vin
  - Fixed (by external resistor) from 0.4V to 1.6V
- I²C version (TPS6286Axx), selection through interface:
  - Output voltage from 0.4V to 1.675V with 5mV step size
  - Power save mode or forced PWM mode
  - Hiccup or latching short-circuit protection
  - Output voltage ramp speed
- Forced PWM or power save mode
- Output voltage discharge
- 100% duty cycle mode
- Hiccup short-circuit protection
- Power-good indicator with window comparator
- Thermal shutdown
- Available in 2mm × 3mm QFN
- Adjustable Soft-start
- –40°C to 125°C operating temperature range
- Create a custom design using the TPS6286Axx and TPS6286Bxx with the WEBENCH® Power Designer

2 Applications

- Core supply for FPGAs, CPUs, ASICs, or video chipsets
- Machine vision cameras
- IP network cameras
- Solid-state drives
- Optical modules

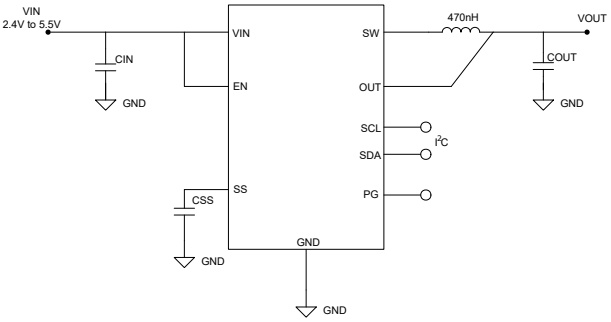
3 Description

The TPS6286Axx and TPS6286Bxx devices are high-frequency, synchronous step-down converters which provide an efficient, flexible, and high power-density design. At medium to heavy loads, the converters operate in pulse width modulation (PWM) mode and automatically enter power save mode operation at light load to maintain high efficiency over the entire load current range. The devices can also be forced in PWM mode operation to minimize output voltage ripple. Together with the DCS-Control architecture, excellent load transient performance and tight output voltage accuracy is achieved. The devices feature a Power-Good signal and an adjustable soft-start feature. The devices are able to operate in 100% mode. For fault protection, the devices incorporate a HICCUP short-circuit protection as well as a thermal shutdown.

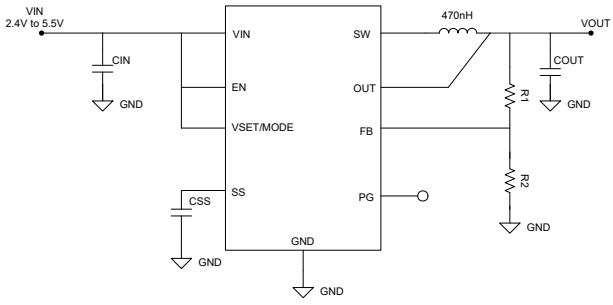
Device Information

PART NUMBER(3)	PACKAGE(1)	PACKAGE SIZE(2)
TPS6286A06	VBM (VQFN-HR, 13)	3mm × 2mm
TPS6286A08(4)		
TPS6286A10(4)		
TPS6286B08(4)		
TPS6286B10		

(1) For more information, see Section 12.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.
(3) See the *Device Options* table.
(4) Preview Information (not Advance Information).



Typical Application Schematic - I²C Version



Typical Application Schematic - FB Version

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4 Device Options

PART NUMBER(1)	OUTPUT VOLTAGE RANGE	START-UP VOLTAGE	OUTPUT CURRENT	VERSION	I²C TARGET ADDRESS
TPS6286A06VBMR	0.4V to Vin	Adjustable or fixed (selectable by external resistor on VSET/MODE)	6A	FB	
TPS6286A08VBMR(1)	0.4V to Vin	Adjustable or fixed (selectable by external resistor on VSET/MODE)	8A	FB	
TPS6286A10VBMR(1)	0.4V to Vin	Adjustable or fixed (selectable by external resistor on VSET/MODE)	10A	FB	
TPS6286B08VBMR(1)	0.4V to 1.675V, 5mV DVS step size through I²C	0.9V	8A	I²C	0x42
TPS6286B10VBMR	0.4V to 1.675V, 5mV DVS step size through I²C	0.9V	10A	I²C	0x42

(1) Preview information (not Advance Information).

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5 Pin Configuration and Functions

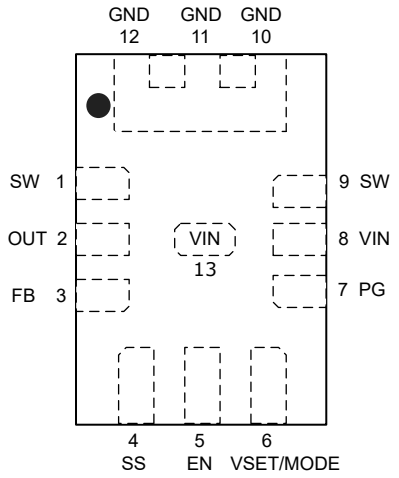

Figure 5-1. 13-Pin VBM VQFN-HR Package for FB Version (Top View)

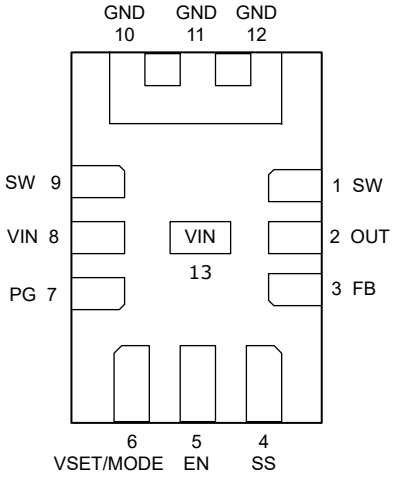

Figure 5-2. 13-Pin VBM VQFN-HR Package for FB Version (Bottom View)

Table 5-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
EN	5	I	Device enable pin. To enable the device, this pin must be pulled high. Pulling this pin low disables the device. Do not leave floating.
FB	3	FB	Voltage feedback input. Connect the output voltage resistor divider to this pin. When using a fixed output voltage, connect directly to OUT.
GND	10,11,12	GND	Power ground pin
OUT	2	I	Output voltage sense pin. This pin must be directly connected to the output capacitor.
PG	7	O	Power-good open-drain output pin. The pullup resistor can be connected to voltages up to 5.5V. If unused, leave this pin floating. This pin is pulled to GND when the device is in shutdown.
SS	4	I	Soft-start pin. An external capacitor can adjust the soft-start time. If unused, leave this pin floating.
SW	1, 9	P	Switch pin of the power stage
VIN	8,13	P	Power supply input voltage pin
VSET/MODE	6	I	Connecting a resistor to GND selects one of the fixed output voltages. Tying the pin high or low selects an adjustable output voltage. After the device has started up, the pin operates as a MODE input. Applying a high level selects forced PWM mode operation and a low level selects power save mode operation.

(1) I = input, O = output, P = power, GND = ground

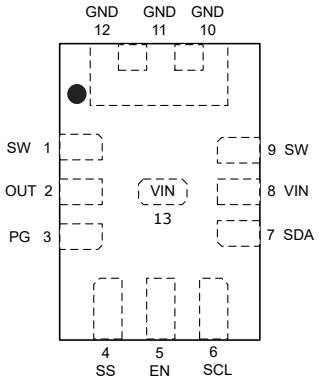

Figure 5-3. 13-Pin VBM VQFN-HR Package for I²C Version (Top View)

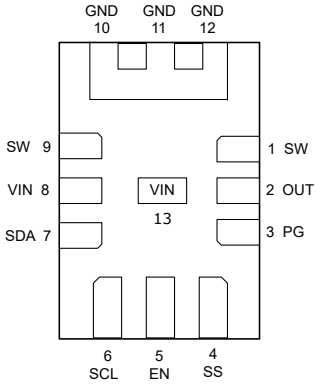

Figure 5-4. 13-Pin VBM VQFN-HR Package for I²C Version (Bottom View)

ADVANCE INFORMATION

Table 5-2. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
EN	5	I	Device enable pin. To enable the device, this pin must be pulled high. Pulling this pin low disables the device. Do not leave floating.
GND	10,11,12	GND	Power ground pin
OUT	2	I	Output voltage sense pin. This pin must be directly connected to the output capacitor.
PG	3	O	Power-good open-drain output pin. The pullup resistor can be connected to voltages up to 5.5V. If unused, leave this pin floating. This pin is pulled to GND when the device is in shutdown.
SCL	6	I	I^2C serial clock pin. Do not leave this pin floating. Connect this pin to AGND if not used.
SDA	7	I/O	I^2C serial data pin. Do not leave this pin floating. Connect this pin to AGND if not used.
SS	4	I	Soft-start pin. An external capacitor can adjust the soft-start time. If unused, leave this pin floating.
SW	1, 9	P	Switch pin of the power stage
VIN	8,13	P	Power supply input voltage pin

(1) I = input, O = output, P = power, GND = ground

6 Specifications

6.1 Absolute Maximum Rating

over operating temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage(2)	VIN, EN, OUT, SDA, SCL, FB, PG, VSET/MODE, SS	–0.3	6	V
	SW (DC)	–0.3	V_{IN} + 0.3	
	SW (AC, less than 10ns)(3)	–2.5	10	
I_{SINK_SDA}	Sink current at SDA		2	mA
I_{SINK_PG}	Sink current at PG		1	mA
T_J	Junction temperature	–40	150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltage values are with respect to network ground terminal.
(3) While switching.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

Over operating junction temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Supply voltage range	2.4		5.5	V
V_{OUT}	Output voltage range, TPS6286Axx	0.4		V_{IN}	V
V_{OUT}	Output Voltage Range, TPS6286Bxx	0.4		1.675	V
V_{IN_SR}	Falling transition time at VIN(1)			10	mV/µs
I_{OUT}	Output current, TPS6286A06			6	A
I_{OUT}	Output current, TPS6286A08, TPS6286B08			8	A
I_{OUT}	Output current, TPS6286A10, TPS6286B10			10	A
T_J	Junction temperature	–40		125	°C

(1) The falling slew rate of V_{IN} must be limited if V_{IN} goes below V_{UVLO}.

6.4 Thermal Information

THERMAL METRIC(1)		TPS6286Axx / TPS6286Bxx		UNIT
		JEDEC 51-7	TPS6286AxxEVM-050 / TPS6286B10EVM-049	
		13 PINS	13 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	71.2	43.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	45.3	n/a(2)	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	16.6	n/a(2)	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	1.7	6.9	°C/W

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6.4 Thermal Information (continued)

THERMAL METRIC(1)		TPS6286Axx / TPS6286Bxx		UNIT
		JEDEC 51-7	TPS6286AxxEVM-050 / TPS6286B10EVM-049	
		13 PINS	13 PINS	
Ψ_{JB}	Junction-to-board characterization parameter	16.6	10.5	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.
(2) Not applicable to an EVM.

6.5 Electrical Characteristics

T_J = –40°C to 125°C, and V_{IN} = 2.4V to 5.5V. Typical values are at T_J = 25°C and V_{IN} = 5V, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
I_{Q_VIN}	Quiescent current	EN = High, no load, device not switching, T_J = 25°C		5.1		µA
I_{Q_OUT}	Operating quiescent current into OUT pin	EN = High, no load, device not switching, V_{OUT} = 1.8V, T_J = 25°C		18		µA
I_{SD}	Shutdown current	EN = Low, T_J = 25°C		0.24	0.6	µA
V_{UVLO}	Undervoltage lock out threshold	V_{IN} rising	2.2	2.3	2.4	V
		V_{IN} falling	2.1	2.2	2.3	V
T_{JSD}	Thermal shutdown threshold	T_J rising		150		°C
	Thermal shutdown hysteresis	T_J falling		20		°C
LOGIC INTERFACE						
V_{IH}	High-level input threshold voltage at EN, SCL, SDA and VSET/MODE		0.9			V
V_{IL}	Low-level input threshold voltage at EN, SCL, SDA and VSET/MODE				0.4	V
$I_{SCL,LKG}$	Input leakage current into SCL pin	T_J = 25°C		0.01	0.2	uA
$I_{SDA,LKG}$	Input leakage current into SDA pin	T_J = 25°C		0.01	0.1	uA
$I_{EN,LKG}$	Input leakage current into EN pin	T_J = 25°C		0.01	0.1	µA
C_{SCL}	Parasictic capacitance at SCL			1		pF
C_{SDA}	Parasictic capacitance at SDA			2.4		pF
STARTUP, POWER GOOD						
t_{Delay}	Enable delay time	Time from EN high to device starts switching 249kΩ resistor connected between VSET/MODE and GND	420	840	1200	µs
t_{Delay}	Enable delay time	Time from EN high to device starts switching, for I^2C devices	100	350	900	us
t_{Ramp}	Output voltage ramp time, TP6286A06	Time from device starts switching to power good (no external capacitor connected)		1.5		ms
t_{Ramp}	Output voltage ramp time, TP6286A08, TPS6286A10, TPS6286B08, TPS6286B10	Time from device starts switching to power good (no external capacitor connected)		0.5		ms
V_{PG}	Power-good lower threshold	V_{OUT} referenced to V_{OUT} nominal	85	91	96	%
	Power-good upper threshold	V_{OUT} referenced to V_{OUT} nominal	103	111	120	%
$V_{PG,OL}$	Low-level output voltage	I_{sink} = 1mA			0.36	V
Iss	SS pin source current			20		µA
$t_{PG,DLY}$	Power-good deglitch delay	Rising and falling edges		34		µs
OUTPUT						
V_{OUT}	Output voltage accuracy	Fixed voltage operation, FPWM, no load, T_J = 25°C	–0.7		0.7	%

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6.5 Electrical Characteristics (continued)

T_J = –40°C to 125°C, and V_{IN} = 2.4V to 5.5V. Typical values are at T_J = 25°C and V_{IN} = 5V, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OUT}	Output voltage accuracy	Fixed voltage operation, FPWM, no load	–1		1	%
V_{FB}	Feedback voltage	Adjustable voltage operation, T_J = 0°C to 85°C	594	600	606	mV
$I_{FB,LKG}$	Input leakage into FB pin	Adjustable voltage operation, V_{FB} = 0.6V, T_J = 25°C		0.01	0.1	µA
R_{DIS}	Output discharge resistor at VOS pin			4.3		Ω
	Load regulation	V_{OUT} = 0.9V, FPWM		0.04		%/A
POWER SWITCH						
$R_{DS(on)}$	High-side FET on-resistance			8		mΩ
	Low-side FET on-resistance			8		mΩ
I_{LIM}	High-side FET forward current limit	TPS6286x06		8		A
I_{LIM}	High-side FET forward current limit	TPS6286x08		11		A
I_{LIM}	High-side FET forward current limit	TPS6286x10		14		A
I_{LIM}	Low-side FET forward current limit	TPS6286x06		6.5		A
I_{LIM}	Low-side FET forward current limit	TPS6286x08		9		A
I_{LIM}	Low-side FET forward current limit	TPS6286x10		12		A
I_{LIM}	Low-side FET negative current limit	TPS6286x06, TPS6286x08, TPS6286x10		–3		A
f_{SW}	PWM switching frequency	I_{OUT} = 1A, V_{OUT} = 0.9V		1.2		MHz

6.6 I²C Interface Timing Characteristics

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$f_{(SCL)}$	SCL clock frequency	Standard mode		100	kHz
		Fast mode		400	kHz
		Fast mode plus		1	MHz
		High-speed mode (write operation), C_B – 100pF max		3.4	MHz
		High-speed mode (read operation), C_B – 100pF max		3.4	MHz
		High-speed mode (write operation), C_B – 400pF max		1.7	MHz
		High-speed mode (read operation), C_B – 400pF max		1.7	MHz
t_{BUF}	Bus free time between a STOP and START condition	Standard mode	4.7		µs
		Fast mode	1.3		µs
		Fast mode plus	0.5		µs
t_{HD}, t_{STA}	Hold time (Repeated) START condition	Standard mode	4		µs
		Fast mode	600		ns
		Fast mode plus	260		ns
		High-speed mode	160		ns
t_{LOW}	LOW period of the SCL clock	Standard mode	4.7		µs
		Fast mode	1.3		µs
		Fast mode plus	0.5		µs
		High-speed mode, C_B – 100pF max	160		ns
		High-speed mode, C_B – 400pF max	320		ns
t_{HIGH}	HIGH period of the SCL clock	Standard mode	4		µs
		Fast mode	600		ns
		Fast mode plus	260		ns
		High-speed mode, C_B – 100pF max	60		ns
		High-speed mode, C_B – 400pF max	120		ns

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6.6 I²C Interface Timing Characteristics (continued)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{SU}, t_{STA}	Setup time for a repeated START condition	Standard mode	4.7		µs
		Fast mode	600		ns
		Fast mode plus	260		ns
		High-speed mode	160		ns
t_{SU}, t_{DAT}	Data setup time	Standard mode	250		ns
		Fast mode	100		ns
		Fast mode plus	50		ns
		High-speed mode	10		ns
t_{HD}, t_{DAT}	Data hold time	Standard mode	0	3.45	µs
		Fast mode	0	0.9	µs
		Fast mode plus	0		µs
		High-speed mode, C_B – 100pF max	0	70	ns
		High-speed mode, C_B – 400pF max	0	150	ns
t_{RCL}	Rise time of SCL signal	Standard mode		1000	ns
		Fast mode	20 + 0.1 C_B	300	ns
		Fast mode plus		120	ns
		High-speed mode, C_B – 100pF max	10	40	ns
		High-speed mode, C_B – 400pF max	20	80	ns
t_{RCL1}	Rise time of SCL signal after a repeated START condition and after an acknowledge BIT	Standard mode	20 + 0.1 C_B	1000	ns
		Fast mode	20 + 0.1 C_B	300	ns
		Fast mode plus		120	ns
		High-speed mode, C_B – 100pF max	10	80	ns
		High-speed mode, C_B – 400pF max	20	160	ns
t_{FCL}	Fall time of SCL signal	Standard mode	20 + 0.1 C_B	300	ns
		Fast mode		300	ns
		Fast mode plus		120	ns
		High-speed mode, C_B – 100pF max	10	40	ns
		High-speed mode, C_B – 400pF max	20	80	ns
t_{RDA}	Rise time of SDA signal	Standard mode		1000	ns
		Fast mode	20 + 0.1 C_B	300	ns
		Fast mode plus		120	ns
		High-speed mode, C_B – 100pF max	10	80	ns
		High-speed mode, C_B – 400pF max	20	160	ns
t_{FDA}	Fall time of SDA signal	Standard mode		300	ns
		Fast mode	20 + 0.1 C_B	300	ns
		Fast mode plus		120	ns
		High-speed mode, C_B – 100pF max	10	80	ns
		High-speed mode, C_B – 400pF max	20	160	ns

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6.6 I²C Interface Timing Characteristics (continued)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$t_{SU,}$ t_{STO}	Setup time of STOP condition	Standard mode	4		µs
		Fast mode	600		ns
		Fast mode plus	260		ns
		High-Speed mode	160		ns
C_B	Capacitive load for SDA and SCL	Standard mode		400	pF
		Fast mode		400	pF
		Fast mode plus		550	pF
		High-Speed mode		400	pF

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6.7 Typical Characteristics

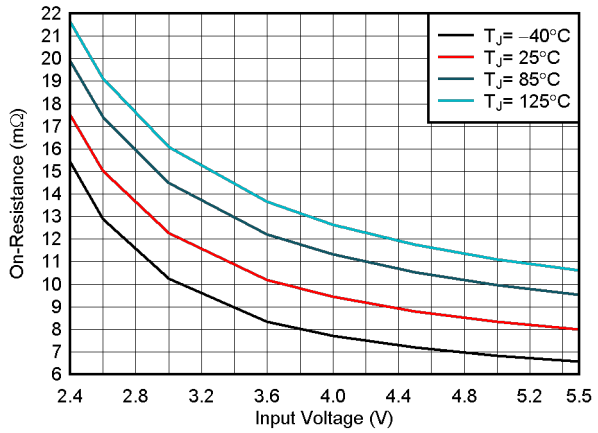

Figure 6-1. High-Side FET On-Resistance $R_{DS(on)}$

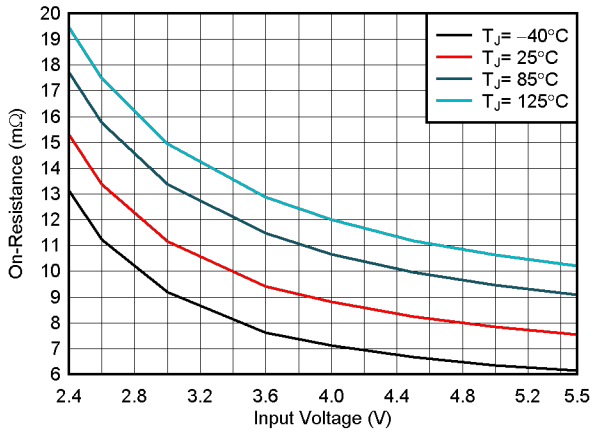

Figure 6-2. Low-Side FET On-Resistance $R_{DS(on)}$

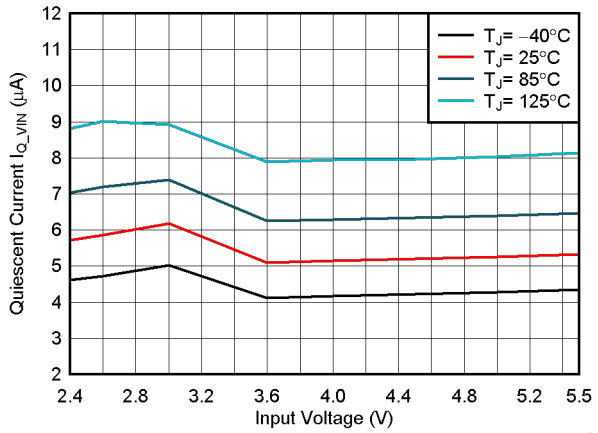

Figure 6-3. Quiescent Current into V_{IN} I_{Q_VIN}

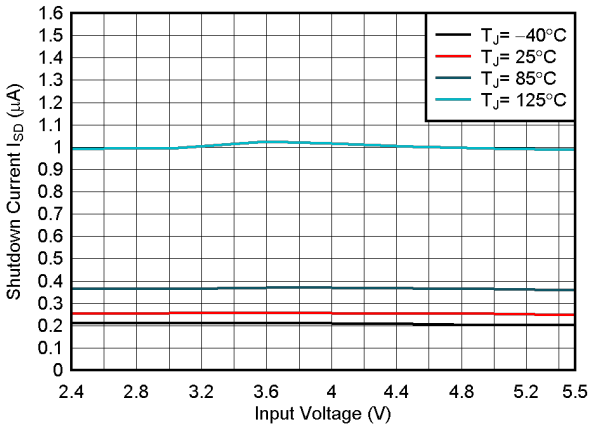

Figure 6-4. Shutdown Current I_{SD}

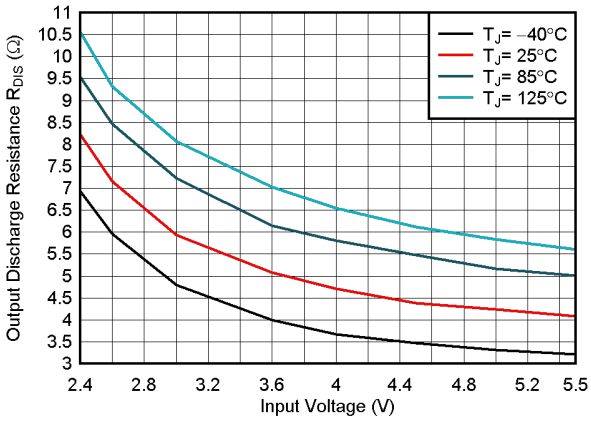

Figure 6-5. Output Discharge Resistance R_{DIS}

7 Detailed Description

7.1 Overview

The TPS6286Axx and TPS6286Bxx synchronous step-down converters use the DCS-Control (Direct Control with seamless transition into power save mode) topology. This topology is an advanced regulation topology that combines the advantages of hysteretic and current-mode control schemes.

The DCS-Control topology operates in PWM (pulse width modulation) mode for medium to heavy load conditions and in power save mode at light load currents. In PWM mode, the converter operates with the 1.2MHz nominal switching frequency, having a controlled frequency variation over the input voltage range. Because DCS-Control supports both PWM and PFM (Pulse Frequency Modulation) within a single building block, the transition from PWM mode to power save mode is seamless and does not affect on the output voltage. The devices offer both excellent DC voltage and load transient regulation combined with very low output voltage ripple.

7.2 Functional Block Diagram

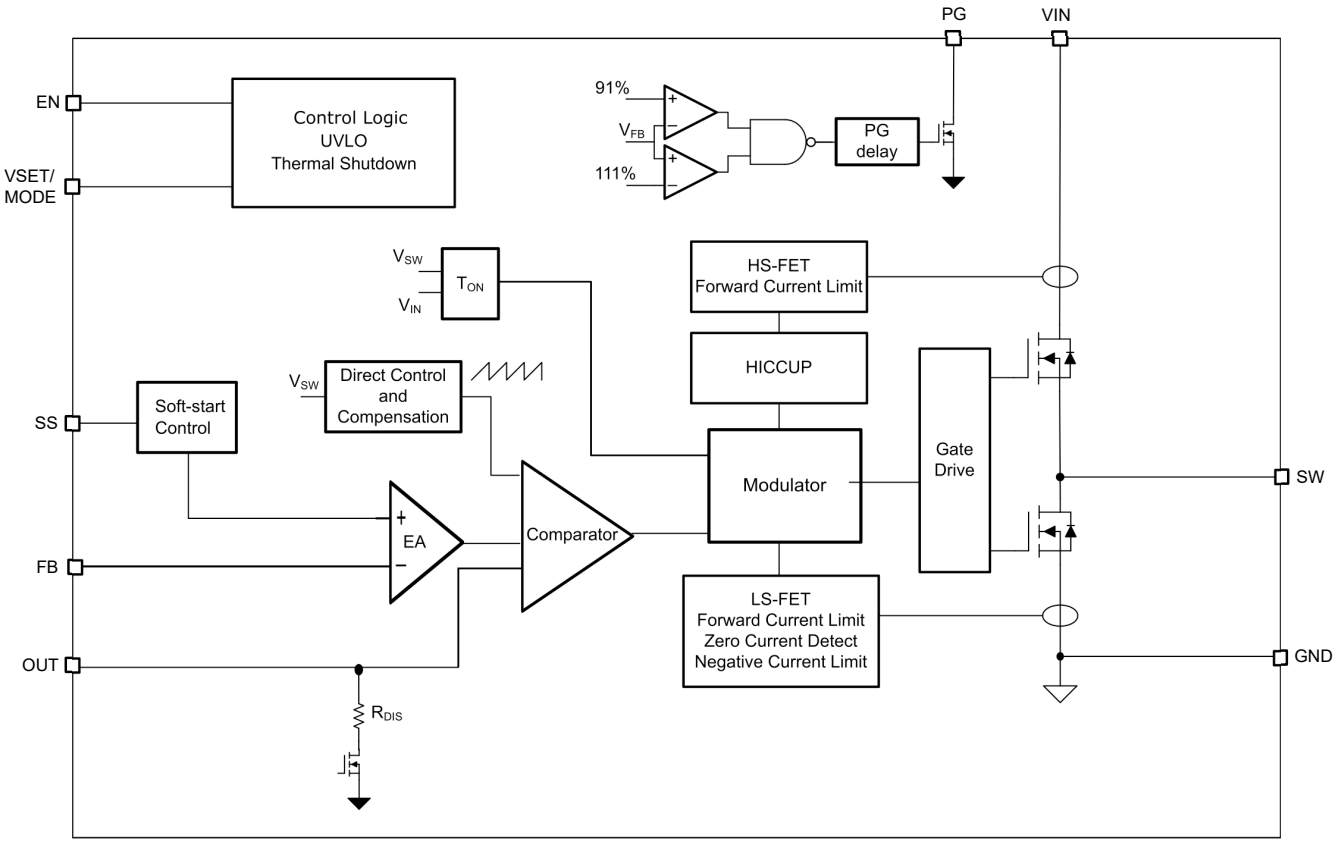

Figure 7-1. Functional Block Diagram- FB version

ADVANCE INFORMATION

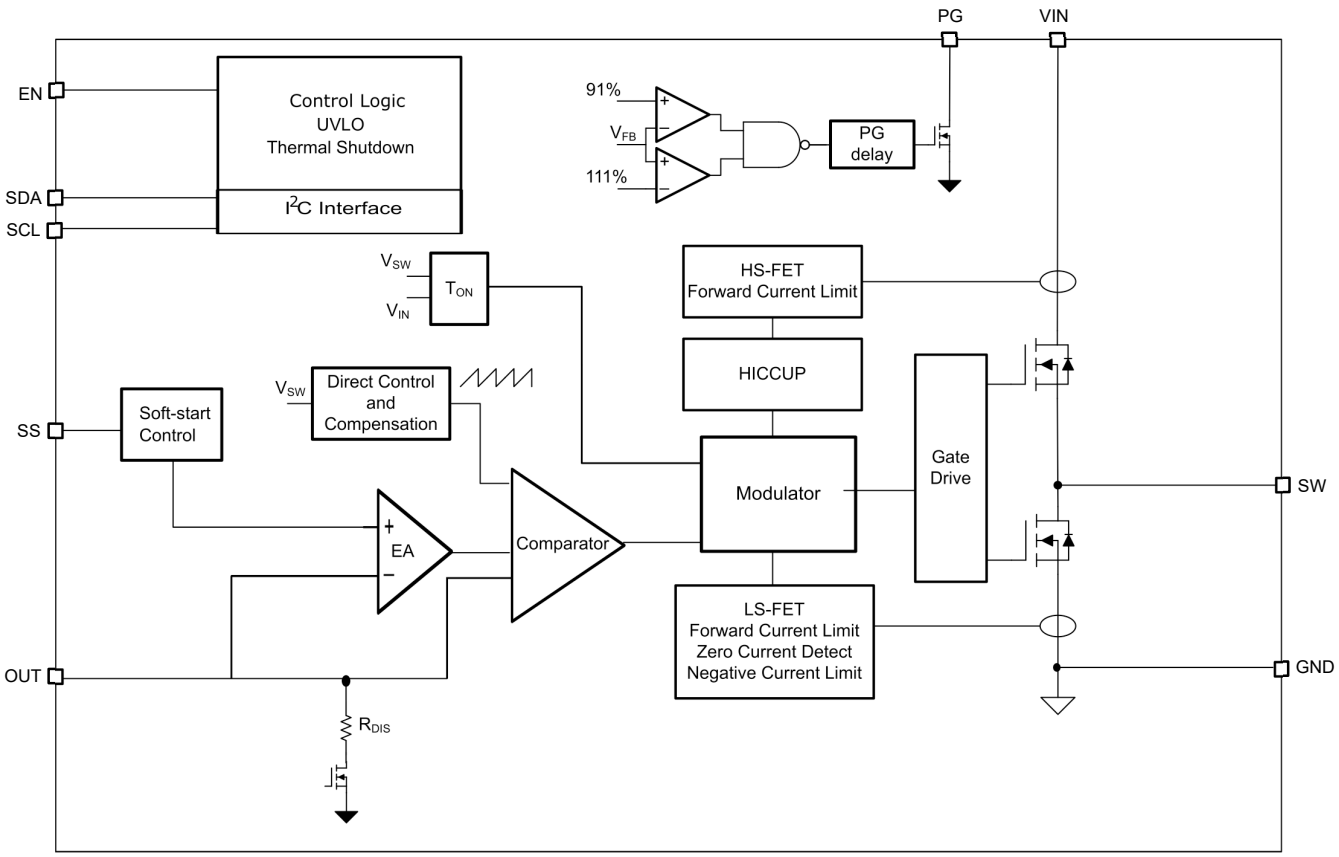

Figure 7-2. Functional Block Diagram- I²C version

7.3 Feature Description

7.3.1 Pulse Frequency Modulation (PFM)

As the load current decreases, the device enters power save mode or pulse frequency modulation (PFM) operation. PFM occurs when the inductor current becomes discontinuous, which is when the inductor current reaches 0A during a switching cycle. Power save mode is based on a fixed on-time architecture, as shown in the following equation.

$$t_{ON} = \frac{V_{OUT}}{V_{IN}} \times 833\ ns \quad (1)$$

In power save mode, the output voltage rises slightly above the nominal output voltage. This effect is minimized by increasing the output capacitor or inductor value.

When V_{IN} decreases to typically 15% above V_{OUT}, the TP6286Axx and TPS6286Bxx does enter power save mode, regardless of the load current. The device maintains output regulation in PWM mode.

7.3.2 Forced PWM Mode

After the device has powered up and ramped up VOUT, the VSET/MODE pin acts as a digital input. With a high level on the VSET/MODE pin, the device enters forced PWM (FPWM) mode and operates with a constant switching frequency over the entire load range, even at very light loads. This reduces the output voltage ripple and allows simple filtering of the switching frequency for noise-sensitive applications but lowers efficiency at light loads.

7.3.3 Low Dropout Operation (100% Duty Cycle)

The device offers a low dropout operation by entering 100% duty cycle mode if the input voltage comes close to the target output voltage. In this mode, the high-side MOSFET switch is constantly turned on. This is particularly

useful in battery-powered applications to achieve the longest operation time by taking full advantage of the whole battery voltage range. The minimum input voltage to maintain a minimum output voltage is given by:

$$V_{IN,MIN} = V_{OUT} + \left(R_{DS(ON)} + R_L\right)I_{OUT,MAX} \quad (2)$$

where

- $V_{IN,MIN}$ is the minimum input voltage to maintain an output voltage.
- $I_{OUT,MAX}$ is the maximum output current.
- $R_{DS(on)}$ is the high-side FET ON-resistance.
- R_L is the inductor ohmic resistance (DCR).

7.3.4 Soft Start

After enabling the device, there is a 700µs (typical) enable delay (t_{delay}) before the device starts switching. After the enable delay, if the SS pin is left un-connected an internal soft start-up circuitry controls the output voltage ramp up with a period of 1.5ms (t_{Ramp}) for TPS6286A06 and with 500us for TP6286A08, TPS6286A10, TPS6286B08, and TPS6286B10. Leaving the SS pin disconnected provides the fastest start-up ramp. This action avoids excessive inrush current and creates a smooth output voltage rise-slope. This action also prevents excessive voltage drops of primary cells and rechargeable batteries with high internal impedance. The device is able to start into a prebiased output capacitor. The device starts with the applied bias voltage and ramps the output voltage to the nominal value. An external soft-start capacitor connected from SS to GND is charged 20µA by an internal current source during soft start until it reaches the reference voltage of 0.9V. The capacitance required to set a certain ramp-time (tramp) therefore is:

$$C_{SS} = \frac{20\mu A \times t_{ramp}[ms]}{0.9V} \quad (3)$$

If the device is set to shutdown (EN = GND), undervoltage lockout, or thermal shutdown, an internal resistor pulls the SS pin to GND to make sure of a proper low level. Returning from those states causes a new start-up sequence.

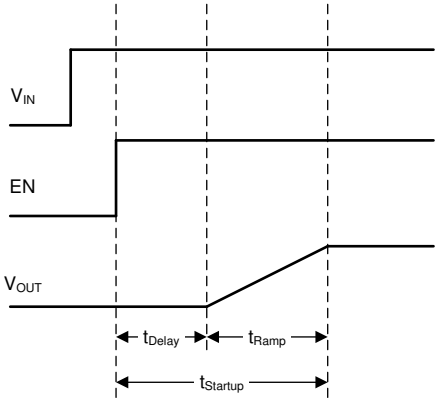

Figure 7-3. Start-up Sequence

7.3.5 Switch Current Limit and HICCUP Short-Circuit Protection

The switch current limit prevents the device from high inductor current and from drawing excessive current from the battery or input voltage rail. Excessive current can occur with a shorted or saturated inductor or a heavy load or shorted output circuit condition. If the inductor current reaches the threshold I_{LIM}, cycle by cycle, the high-side MOSFET is turned off and the low-side MOSFET is turned on, while the inductor current ramps down to the low-side MOSFET current limit.

When the high-side MOSFET current limit is triggered 32 times, the device stops switching. The device then automatically restarts with an internal soft start-up after a typical delay time of 128µs has passed. This action is named HICCUP short-circuit protection. The device repeats this mode until the high load condition disappears.

The HICCUP is disabled by the CONTROL register bit Enable HICCUP. Disabling HICCUP changes the overcurrent protection to latching protection. The device stops switching after the high-side MOSFET current limit is triggered 32 times. Toggling the EN pin, removing and reapplying the input voltage, or writing to the CONTROL register bit Software Enable Device unlatches the device.

7.3.6 Undervoltage Lockout

To avoid misoperation of the device at low input voltages, undervoltage lockout (UVLO) is implemented when the input voltage is lower than V_{UVLO}. The device stops switching and the output voltage discharge is active when the device is in UVLO. When the input voltage recovers, the device automatically returns to operation with an internal soft start-up.

The UVLO bit in the STATUS Register is set when the input voltage is less than the UVLO falling threshold. When the input voltage is below 1.8V (typical), all registers are reset.

7.3.7 Thermal Warning and Shutdown

When the junction temperature goes up to TJW, the device gives a pre-warning indicator in the STATUS register. The device keeps running. When the junction temperature exceeds T_{JSD}, the device goes into thermal shutdown, stops switching, and activates the output voltage discharge. When the device temperature falls below the threshold by the hysteresis, the device returns to normal operation automatically with an internal soft start-up. During thermal shutdown, the internal register values are kept.

7.4 Device Functional Modes

7.4.1 Enable and Disable (EN)

The device is enabled by setting the EN pin to a logic high. In shutdown mode (EN = low), the internal power switches and the entire control circuitry are turned off. An internal switch smoothly discharges the output through the VOS pin in shutdown mode. Do not leave the EN pin floating.

7.4.2 Output Discharge

The purpose of the output discharge function is to make sure of a defined down-ramp of the output voltage when the device is disabled and to keep the output voltage close to 0V. The output discharge is active when the enable output discharge bit is set to 1 and the EN pin is pulled low, when the Input voltage is below the UVLO threshold, or during thermal shutdown. The discharge is active down to an input voltage of 1.6V (typical). The enable output discharge bit is reset on the rising edge of the EN pin.

7.4.3 Power Good (PG)

The device has an open-drain power-good pin, which is specified to sink up to 1mA. The power-good output requires a pullup resistor connecting to any voltage rail less than 5.5V. The PG has a deglitch delay of 34µs.

The PG signal can be used for sequencing of multiple rails by connecting the PG signal to the EN pin of other converters. Leave the PG pin unconnected when not used.

Table 7-1. PG Function Table

DEVICE CONDITIONS		PG PIN
Enable	$0.9 \times V_{OUT\_NOM} \le V_{VOS} \le 1.1 \times V_{OUT\_NOM}$	Hi-Z
	$V_{VOS} < 0.9 \times V_{OUT\_NOM}$ or $V_{VOS} > 1.1 \times V_{OUT\_NOM}$	Low
Shutdown	EN = low	Low
Thermal shutdown	$T_J > T_{JSD}$	Low
UVLO	$1.8V < V_{IN} < V_{UVLO}$	Low
Power supply removal	$V_{IN} < 1.8V$	Undefined

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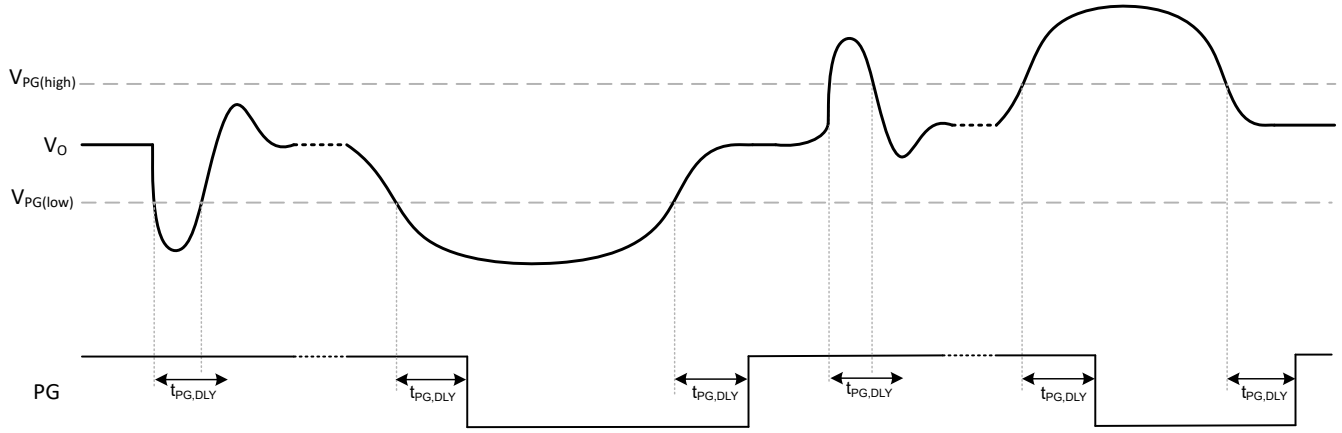

Figure 7-4. Power-Good Transient and Delay Behavior

7.4.4 Voltage Setting and Mode Selection (VSET/MODE)

During the enable delay (t_{Delay}), the device configuration is set by an external resistor connected to the VSET/MODE pin through an internal R2D (resistor to digital) converter. Table 7-2 shows the options.

The R2D converter has an internal current source that applies current through the external resistor and an internal ADC that reads back the resulting voltage level. Depending on the level, the output voltage is set. After this R2D conversion is finished, the current source is turned off to avoid current flowing through the external resistor. Make sure that there is no additional current path or capacitance greater than 30pF from this pin to GND during R2D conversion. Otherwise, a false value is set.

Table 7-2. Voltage Selection Table

RESISTOR (E96 SERIES, ±1% ACCURACY) AT VSET/MODE PIN	FIXED OR ADJUSTABLE OUTPUT VOLTAGE
249kΩ or logic high	Adjustable (through a resistive divider on the FB pin)
205kΩ	1.60V
162kΩ	1.50V
133kΩ	1.35V
105kΩ	1.20V
86.6kΩ	Reserved
68.1kΩ	1.00V
56.2kΩ	0.90V
44.2kΩ	0.85V
36.5kΩ	0.80V
28.7kΩ	0.70V
23.7kΩ	0.60V
18.7kΩ	0.50V
15.4kΩ	0.45V
12.1kΩ	0.40V
10kΩ or logic low	Adjustable (through a resistive divider on the FB pin)

When the device is set as a fixed output voltage converter, then FB pin must be connected to the output directly. Refer to Figure 7-5.

After the start-up period ($t_{Startup}$), a different operation mode can be selected. When VSET/MODE is high, the device operates in forced PWM mode, otherwise the device operates in power save mode.

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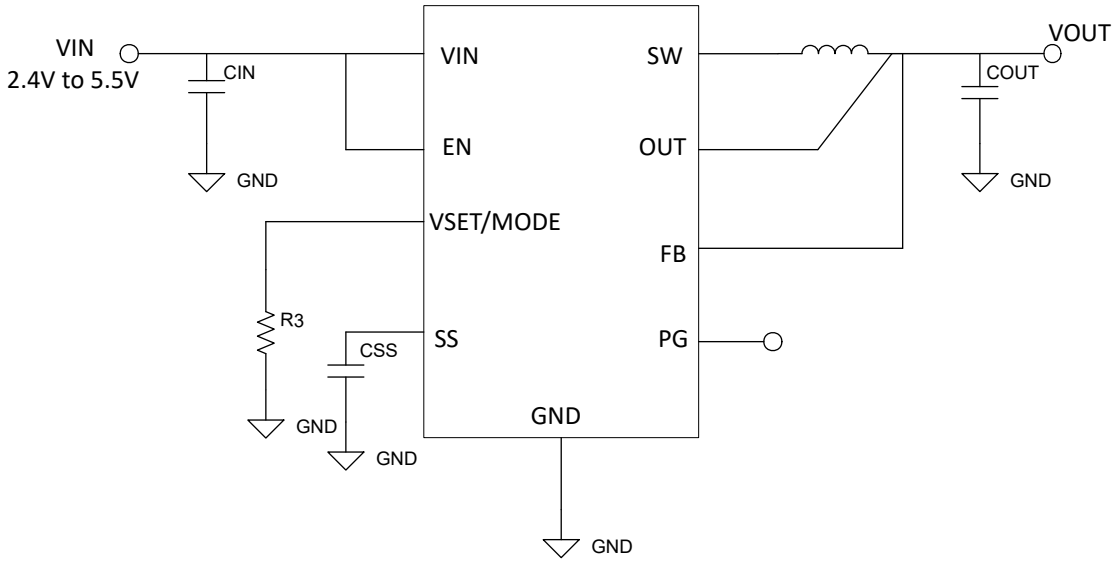

Figure 7-5. Typical Application - Fixed Start-up Output Voltage

7.5 Programming

7.5.1 Serial Interface Description

I²C is a 2-wire serial interface developed by Philips Semiconductor, now NXP Semiconductors. The bus consists of a data line (SDA) and a clock line (SCL) with pullup structures. When the bus is *idle*, both SDA and SCL lines are pulled high. All the I²C-compatible devices connect to the I²C bus through open drain I/O pins, SDA and SCL. A *controller* device, usually a microcontroller or a digital signal processor, controls the bus. The controller is responsible for generating the SCL signal and device addresses. The controller also generates specific conditions that indicate the START and STOP of data transfer. A *target* device receives or transmits data on the bus under control of the controller device, or both.

The device works as a *target* and supports the following data transfer *modes*, as defined in the I²C-Bus Specification: standard mode (100kbps) and fast mode (400kbps), fast mode plus (1Mbps), and high-speed mode (3.4Mbps). The interface adds flexibility to the power supply design, enabling most functions to be programmed to new values depending on the instantaneous application requirements. Register contents remain intact as long as the input voltage remains above 1.8V.

The data transfer protocol for standard and fast modes is exactly the same, therefore, the modes are referred to as F/S mode in this document. The protocol for high speed mode is different from F/S mode, and the mode referred to as HS mode.

TI recommends that the I²C controller initiates a STOP condition on the I²C bus after the initial power up of SDA and SCL pullup voltages to make sure of a reset of the I²C engine.

7.5.2 Standard-, Fast-, and Fast-Mode Plus Protocol

The controller initiates data transfer by generating a start condition. The start condition is when a high-to-low transition occurs on the SDA line while SCL is high, as shown in Figure 7-6. All I²C-compatible devices recognize a start condition.

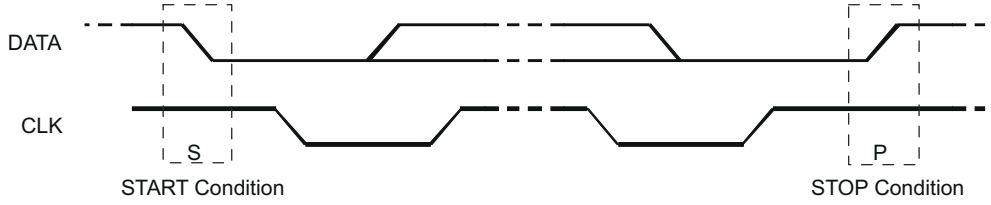

Figure 7-6. START and STOP Conditions

The controller then generates the SCL pulses and transmits the 7-bit address and the read, write direction bit R/$\overline{W}$ on the SDA line. During all transmissions, the controller makes sure that data is valid. A valid data condition requires the SDA line to be stable during the entire high period of the clock pulse (see Figure 7-7). All devices recognize the address sent by the controller and compare to the internal fixed addresses. Only the target device with a matching address generates an acknowledge (see Figure 7-8) by pulling the SDA line low during the entire high period of the ninth SCL cycle. Upon detecting this acknowledge, the controller knows that communication link with a target has been established.

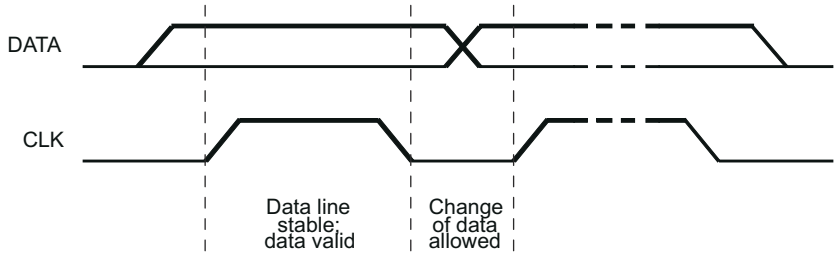

Figure 7-7. Bit Transfer on the Serial Interface

The controller generates further SCL cycles to either transmit data to the target (R/$\overline{W}$ bit 0) or receive data from the target (R/$\overline{W}$ bit 1). In either case, the receiver needs to acknowledge the data sent by the transmitter. So an acknowledge signal can either be generated by the controller or by the target, depending on which one is the receiver. 9-bit valid data sequences consisting of 8-bit data and 1-bit acknowledge can continue as long as necessary.

To signal the end of the data transfer, the controller generates a stop condition by pulling the SDA line from low to high while the SCL line is high (see Figure 7-6). This action releases the bus and stops the communication link with the addressed target. All I^2C compatible devices must recognize the stop condition. Upon the receipt of a stop condition, all devices know that the bus is released, and the devices wait for a start condition followed by a matching address.

Attempting to read data from register addresses not listed in this section results in 0x00 being read out.

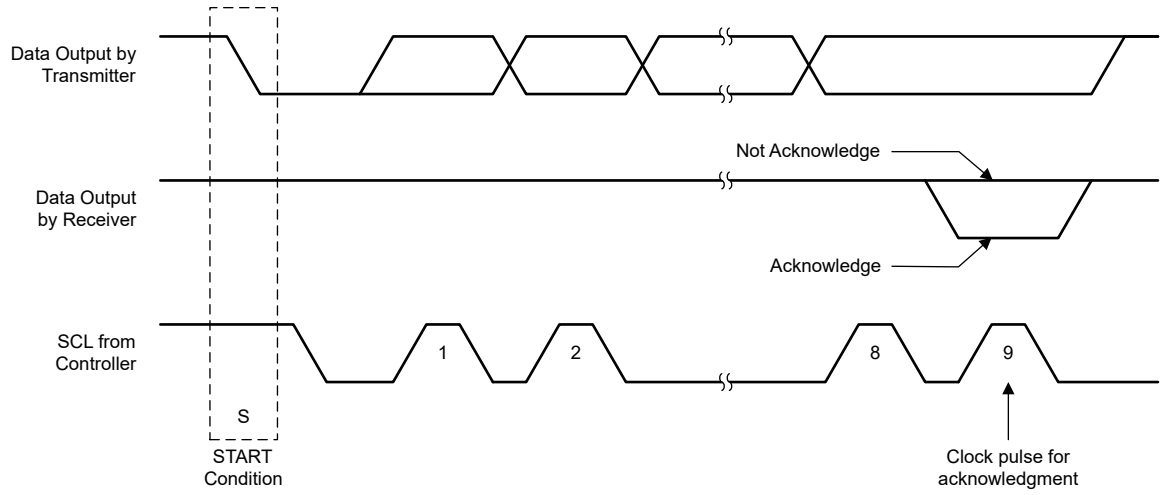

Figure 7-8. Acknowledge on the I^2C Bus

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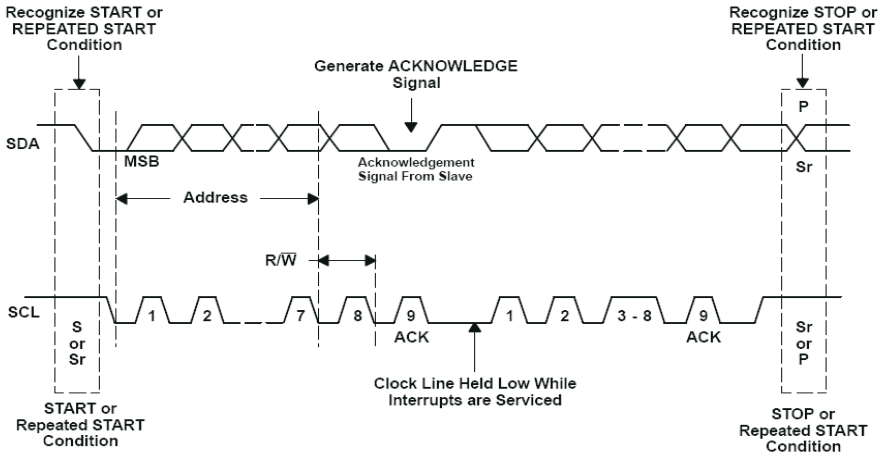

Figure 7-9. Bus Protocol

7.5.3 HS Mode Protocol

The controller generates a start condition followed by a valid serial byte containing HS controller code 00001XXX. This transmission is made in F/S-mode at no more than 400kbps. No device is allowed to acknowledge the HS controller code, but all devices must recognize the HS controller code and switch the internal setting to support 3.4Mbps operation.

The controller then generates a *repeated start condition* (a repeated start condition has the same timing as the start condition). After this repeated start condition, the protocol is the same as F/S-mode, except that transmission speeds up to 3.4Mbps are allowed. A stop condition ends the HS mode and switches all the internal settings of the target devices to support the F/S mode. Instead of using a stop condition, repeated start conditions must be used to secure the bus in HS-mode.

Attempting to read data from register addresses not listed in this section results in 0x00 being read out.

7.5.4 I²C Update Sequence

The sequence requires a start condition, a valid I²C target address, a register address byte, and a data byte for a single update. After the receipt of each byte, the device acknowledges by pulling the SDA line low during the high period of a single clock pulse. A valid I²C address selects the device. The device performs an update on the falling edge of the acknowledge signal that follows the LSB byte.

Figure 7-10. "Write" Data Transfer Format in Standard-, Fast, and Fast-Plus Modes

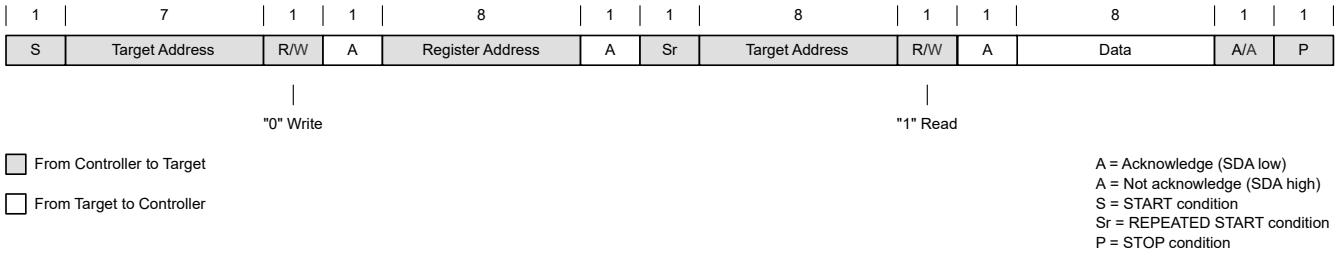

Figure 7-11. "Read" Data Transfer Format in Standard-, Fast, and Fast-Plus Modes

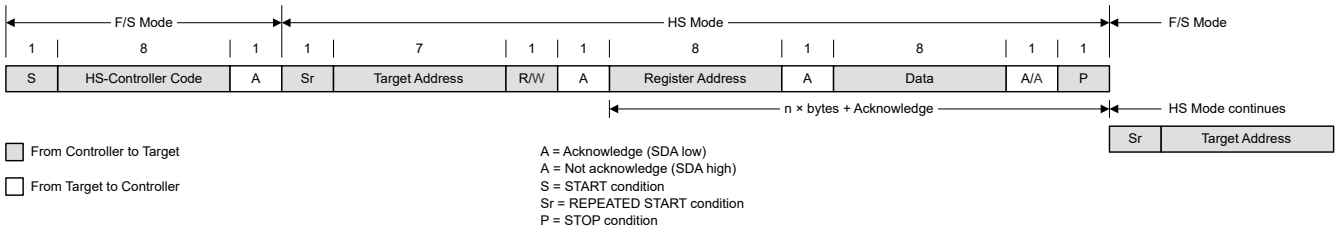

Figure 7-12. Data Transfer Format in HS-Mode

7.5.5 I²C Register Reset

The I²C registers can be reset by:

- Pulling the input voltage below 1.8V (typical)
- A high to low transition on EN
- Setting the Reset bit in the CONTROL register. When Reset is set to 1, all registers are reset to the default values and a new start-up is begun immediately. After t_{Delay}, the I²C registers can be programmed again.

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8 Register Map

Table 8-1. Register Map

REGISTER ADDRESS (HEX)	REGISTER NAME	FACTORY DEFAULT (HEX)	DESCRIPTION
0x01	V_{OUT} Register 1	0x64	Sets the target output voltage
0x02	V_{OUT} Register 2	0x64	Sets the target output voltage
0x03	CONTROL Register	0x6F	Sets miscellaneous configuration bits
0x05	STATUS Register	0x00	Returns status flags

8.1 Target Address Byte

7	6	5	4	3	2	1	0
1	x	x	x	x	x	x	R/$\overline{W}$

The target address byte is the first byte received following the START condition from the controller device.

8.2 Register Address Byte

7	6	5	4	3	2	1	0
0	0	0	0	0	D2	D1	D0

Following the successful acknowledgment of the target address, the bus controller sends a byte to the device, which contains the address of the register to be accessed.

8.3 V_{OUT} Register 1

Table 8-2. V_{OUT} Register 1 Description

REGISTER ADDRESS 0X01 READ/WRITE			
BIT	FIELD	VALUE (HEX)	OUTPUT VOLTAGE (TYPICAL)
7:0	VO1_SET	0x00	400mV
		0x01	405mV
		...	
		0x64	900mV
		...	
		0xFE	1670mV
		0xFF	1675mV

8.4 V_{OUT} Register 2

Table 8-3. V_{OUT} Register 2 Description

REGISTER ADDRESS 0X02 READ/WRITE			
BIT	FIELD	VALUE (HEX)	OUTPUT VOLTAGE (TYPICAL)
7:0	VO2_SET	0x00	400mV
		0x01	405mV
		...	
		0x64	**900mV** (default value)
		...	
		0xFE	1670mV
		0xFF	1675mV

8.5 CONTROL Register

Table 8-4. CONTROL Register Description

REGISTER ADDRESS 0X03 WRITE ONLY				
BIT	**FIELD**	**TYPE**	**DEFAULT**	**DESCRIPTION**
7	Reset	R/W	0	1 - Reset all registers to default.
6	Enable FPWM Mode during Output Voltage Change	R/W	1	0 - Keep the current mode status during output voltage change 1 - Force the device in FPWM during output voltage change.
5	Software Enable Device	R/W	1	0 - Disable the device. All registers values are still kept. 1 - Re-enable the device with a new start-up without the t_{Delay} period.
4	Enable FPWM Mode	R/W	0	0 - Set the device in power save mode at light loads. 1 - Set the device in forced PWM mode at light loads.
3	Enable Output Discharge	R/W	1	0 - Disable output discharge. 1 - Enable output discharge.
2	Enable HICCUP	R/W	1	0 - Disable HICCUP. Enable latching protection. 1 - Enable HICCUP, Disable latching protection.
0:1	Voltage Ramp Speed	R/W	11	00 - 20mV/µs (0.25µs/step) 01 - 10mV/µs (0.5µs/step) 10 - mV/µs (1µs/step) 11 - 1mV/µs (5µs/step, default)

8.6 STATUS Register

Table 8-5. STATUS Register Description

REGISTER ADDRESS 0X05 READ ONLY(1)				
BIT	**FIELD**	**TYPE**	**DEFAULT**	**DESCRIPTION**
7:5	Reserved			
4	Thermal Warning	R	0	1: Junction temperature is higher than 130°C.
3	HICCUP	R	0	1: Device has HICCUP status once.
2	Reserved			
1	Reserved			
0	UVLO	R	0	1: The input voltage is less than UVLO threshold (falling edge).

(1) All bit values are latched until the device is reset, or the STATUS register is read. Then, the STATUS register is reset to the default values.

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9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The following section discusses the design of the external components to complete the power supply design for several input and output voltage options by using typical applications as a reference.

9.2 Typical Application

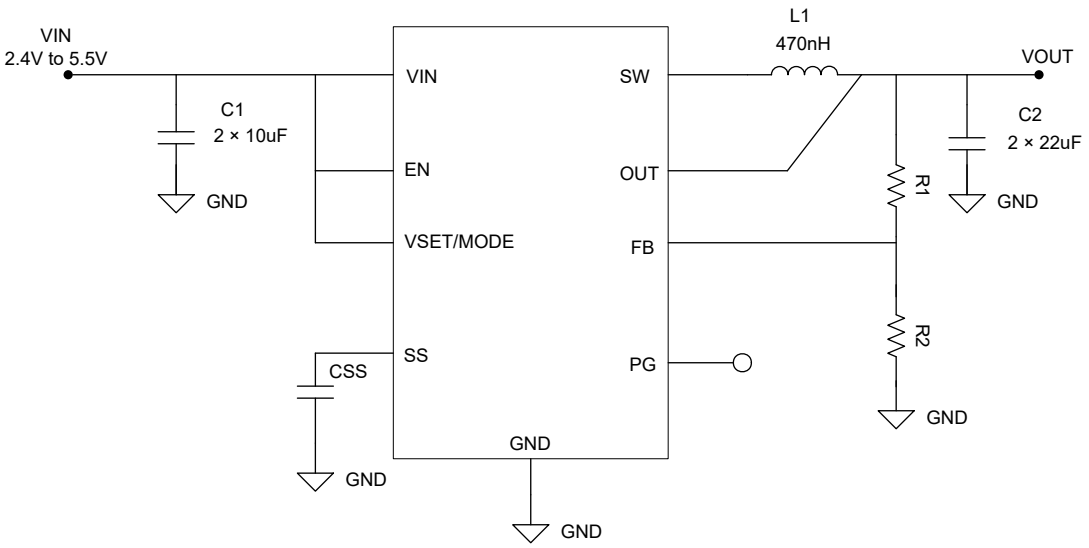

Figure 9-1. Typical Application Circuit- TPS6286A06

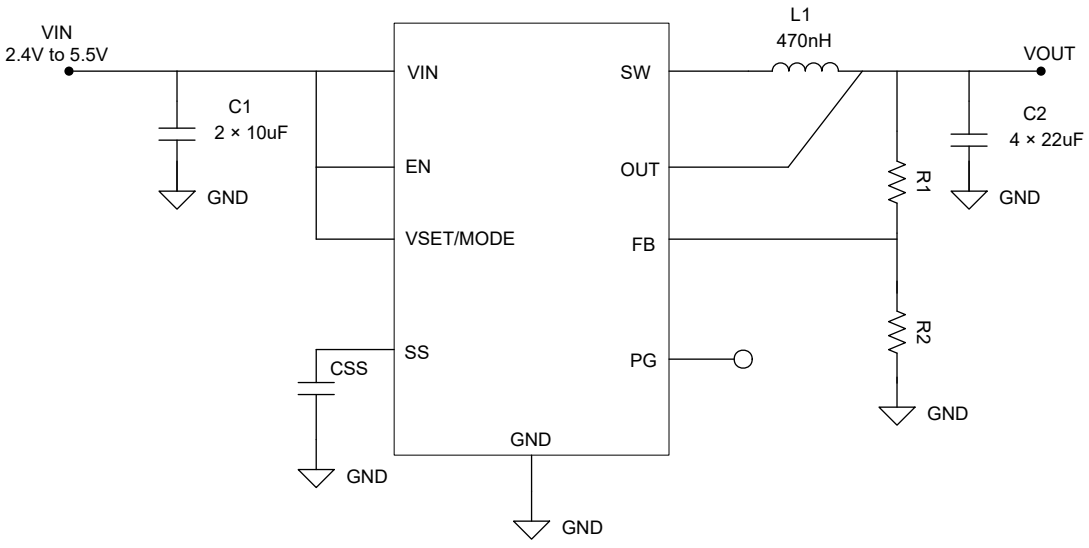

Figure 9-2. Typical Application Circuit- TPS6286A10

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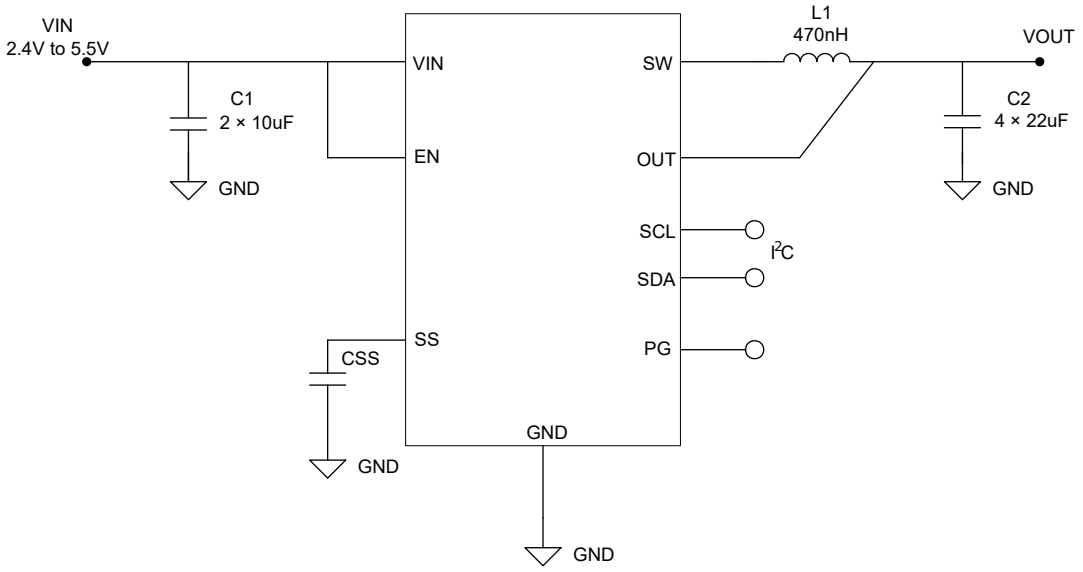

Figure 9-3. Typical Application Circuit- TPS6286B10

9.2.1 Design Requirements

For this design example, use the parameters listed in Table 9-1 as the input parameters.

Table 9-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage	2.4V to 5.5V
Output voltage	1.2V
Maximum output current	10A

Table 9-2 lists the components used for the example.

Table 9-2. List of Components

REFERENCE	DESCRIPTION	MANUFACTURER(1)
C1	CAP, CERM, 10uF, 10V, +/– 10%, X7R, 0805, GCM21BR71A106KE22L	MURATA
C2	CAP, CERM, 22uF, 10V, +/– 20%, X7R, 0805, GRM21BZ71A226ME15L	MURATA
L1	470 nH Shielded Molded Inductor 16A 4.3mOhm Max Nonstandard, XGL5020-471MEC	Coilcraft
CSS	Internal SS time as per the electrical characteristics table. To be populated as per the desired soft-start time.	Any
R1	100kΩ, chip resistor, 1/16 W, 1%, size 0402	Std
R2	100kΩ, chip resistor, 1/16 W, 1%, size 0402	Std

(1) See the *Third-Party Products* disclaimer.

9.2.2 Detailed Design Procedure

9.2.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the TPS6286A10, TPS6286A08 and TPS6286A06 devices with the WEBENCH® Power Designer.

Click here to create a custom design using the TPS6286B10 and TPS6286A08 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

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The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

9.2.2.2 Setting The Output Voltage

The output voltage is set by an external resistor divider according to the following equation:

$$R1 = R2\left(\frac{V_{OUT}}{V_{FB}} - 1\right) = R2\left(\frac{V_{OUT}}{0.6V} - 1\right) \quad (4)$$

R2 must not be higher than 200kΩ to achieve high efficiency at light load while providing acceptable noise sensitivity.

For the fixed output versions, connect the FB pin to the output. R1 and R2 are not needed.

9.2.2.3 Output Filter Design

The inductor and the output capacitor together provide a low-pass filter. To simplify this process, Table 9-3 outlines possible inductor and capacitor value combinations for most applications. Checked cells represent combinations that are proven for stability by simulation and lab testing. Further combinations must be checked for each individual application.

Table 9-3. Matrix of Output Capacitor and Inductor Combinations for TPS6286A06

NOMINAL L [µH](2)	NOMINAL C_{OUT} [µF](3)		
	2 × 22 or 47	3 × 22	150
0.47	+(1)	+	+

(1) This LC combination is the standard value and recommended for most applications.
(2) Inductor tolerance and current derating is anticipated. The effective inductance can vary by 20% and –30%.
(3) Capacitance tolerance and bias voltage derating is anticipated. The effective capacitance can vary by 20% and –50%.

Table 9-4. Matrix of Output Capacitor and Inductor Combinations for TPS6286A08 and TPS6286A10

NOMINAL L [µH](2)	NOMINAL C_{OUT} [µF](3)		
	4 × 22 or 2 × 47	3 × 47	150
0.47	+(1)	+	+

(1) This LC combination is the standard value and recommended for most applications.
(2) Inductor tolerance and current derating is anticipated. The effective inductance can vary by 20% and –30%.
(3) Capacitance tolerance and bias voltage derating is anticipated. The effective capacitance can vary by 20% and –50%.

9.2.2.4 Inductor Selection

The main parameter for the inductor selection is the inductor value, then the saturation current of the inductor. To calculate the maximum inductor current under static load conditions, the following equations are given.

$$I_{L,MAX} = I_{OUT,MAX} + \frac{\Delta I_L}{2} \quad (5)$$

$$\Delta I_L = V_{OUT}\left(\frac{1 - \frac{V_{OUT}}{V_{IN}}}{L \times f_{SW}}\right) \quad (6)$$

where

- $I_{OUT,MAX}$ is the maximum output current

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- ΔI_L is the inductor current ripple
- f_{SW} is the switching frequency
- L is the inductor value

TI recommends to choose a saturation current for the inductor that is approximately 20% to 30% higher than $I_{L,MAX}$. In addition, DC resistance and size must also be taken into account when selecting an appropriate inductor. Table 9-5 lists recommended inductors.

Table 9-5. List of Recommended Inductors

INDUCTANCE [µH] (1)	CURRENT RATING [A]	DIMENSIONS [L × W × H mm]	DC RESISTANCE [mΩ]	PART NUMBER	Notes
0.47	15.7	5.48 × 5.28 × 2	3.7	Coilcraft, XGL5020-471ME	For I_{OUT}> 6A
0.47	17.1	4.3 × 4.3 × 3	3.9	Wuerth Elektronik, 744393240047	For I_{OUT}> 6A
0.47	13.4	4 × 4 × 2	4.2	Coilcraft, XGL4020-471ME	For I_{OUT}≤ 6A
0.47	12.7	4.1 × 4.1 × 2	7	Wuerth Elektronik, 744383560047HT	For I_{OUT}≤ 6A

(1) See the *Third-Party Products* disclaimer.

9.2.2.5 Capacitor Selection

The input capacitor is the low-impedance energy source for the converters, which helps to provide stable operation. TI recommends a low-ESR multilayer ceramic capacitor for the best filtering and must be placed between VIN and GND as close as possible to those pins. For most applications, 10µF of *effective* [1] capacitance is sufficient, however, a larger value reduces input current ripple.

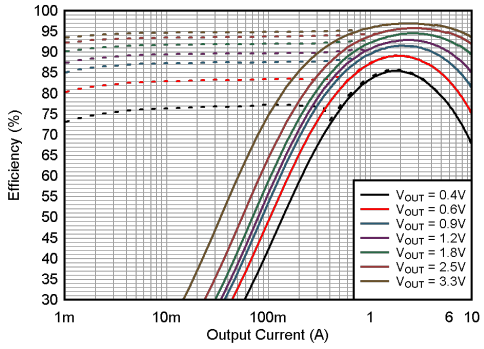
The architecture of the device allows the use of tiny ceramic output capacitors with low equivalent series resistance (ESR). These capacitors provide low output voltage ripple and are recommended. To keep the low resistance up to high frequencies and to get narrow capacitance variation with temperature, TI recommends using X7R or X5R dielectrics. For operations up to 6A output current, the recommended typical output capacitor value is 30µF of *effective* capacitance. For operations up to 10A output current, the recommended typical output capacitor value is 55µF of *effective* capacitance. Values over 200µF can degrade the loop stability of the converter.

ADVANCE INFORMATION

[1] The effective capacitance is the capacitance after tolerance, temperature, and DC bias effects have been considered.

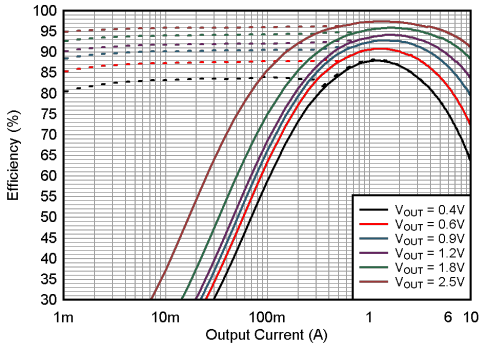
9.2.3 Application Curves

V_{IN} = 5.0V, V_{OUT} = 1.2V, T_A = 25°C, BOM = Table 9-2, unless otherwise noted. Solid lines show the FPWM mode and dashed lines show PFM.



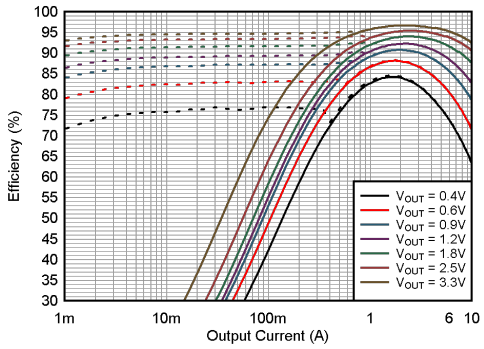
V_{IN}= 5V T_A = 25°C PFM and FPWM

Figure 9-4. Efficiency versus Output Current



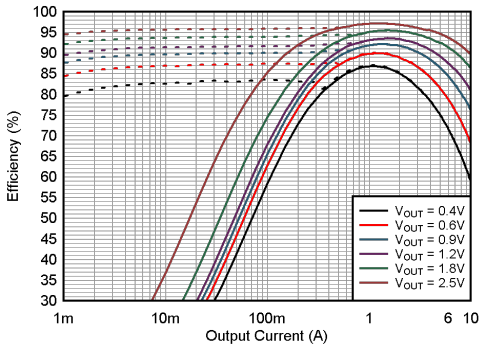
V_{IN}= 3.3V T_A = 25°C PFM and FPWM

Figure 9-5. Efficiency versus Output Current



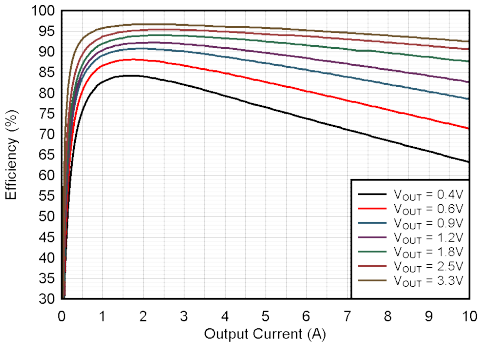
V_{IN}= 5V T_A = 85°C PFM and FPWM

Figure 9-6. Efficiency versus Output Current



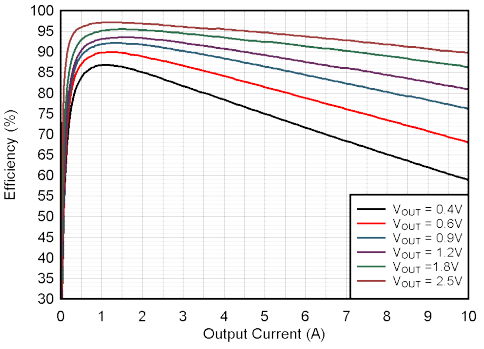
V_{IN}= 3.3V T_A = 85°C PFM and FPWM

Figure 9-7. Efficiency versus Output Current



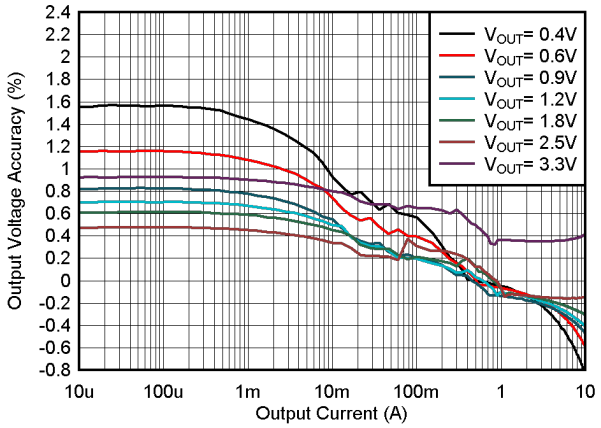
V_{IN}= 5V T_A = 85°C FPWM

Figure 9-8. Efficiency versus Output Current



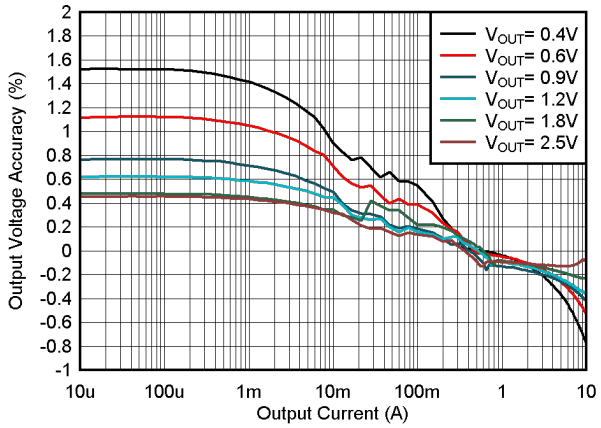
V_{IN}= 3.3V T_A = 85°C FPWM

Figure 9-9. Efficiency versus Output Current



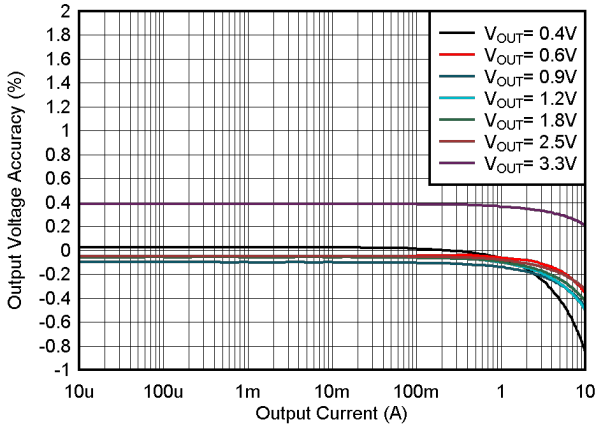
V_{IN}= 5V T_A = 25°C PFM

Figure 9-10. Load Regulation



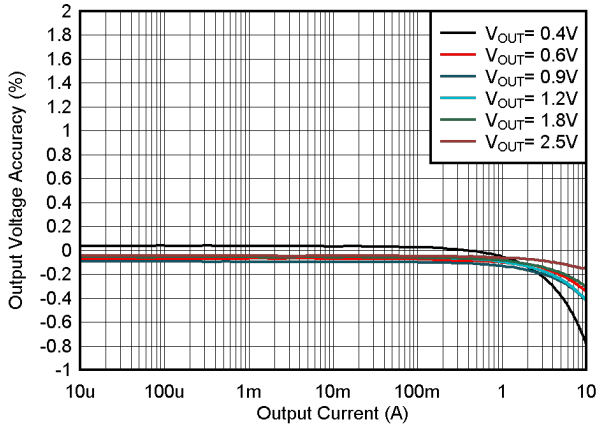
V_{IN}= 3.3V T_A = 25°C PFM

Figure 9-11. Load Regulation



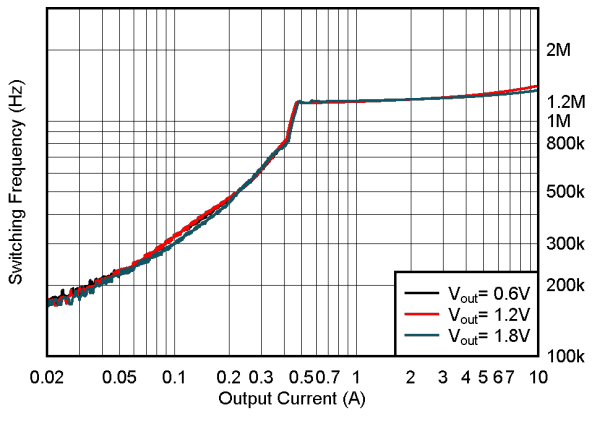
V_{IN}= 5V T_A = 25°C FPWM

Figure 9-12. Load Regulation



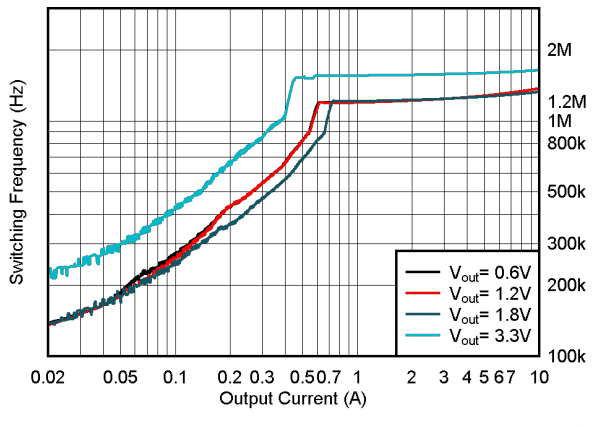
V_{IN} = 3.3V T_A = 25°C FPWM

Figure 9-13. Load Regulation



V_{IN} = 3.3V T_A = 25°C PFM

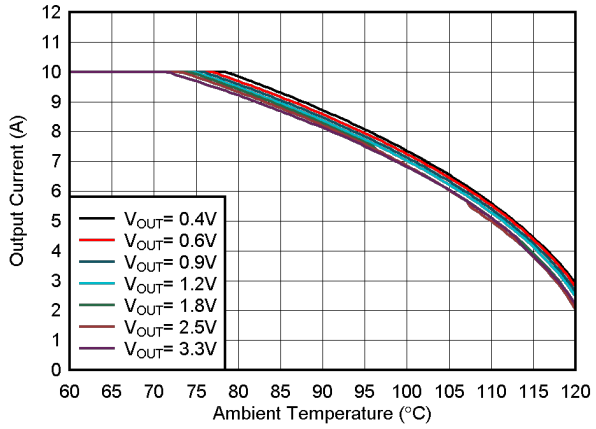
Figure 9-14. Switching Frequency



V_{IN} = 5.0V T_A = 25°C PFM

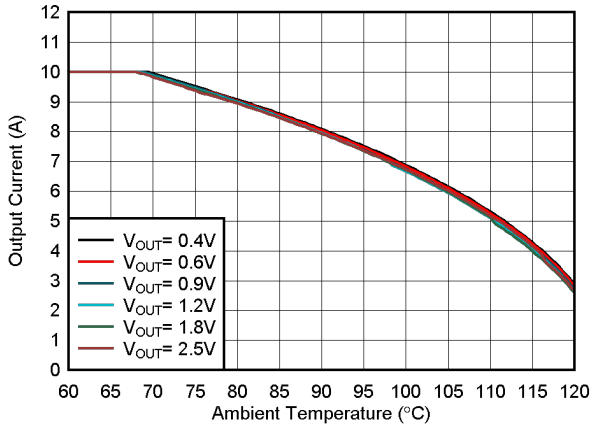
Figure 9-15. Switching Frequency

ADVANCE INFORMATION



V_{IN} = 5.0V $R_{\theta JA}$ = 43.2°C/W T_{JMAX}= 125°C

Figure 9-16. Safe Operating Area



V_{IN} = 3.3V $R_{\theta JA}$ = 43.2°C/W T_{JMAX}= 125°C

Figure 9-17. Safe Operating Area

V_{IN} = 2.4V to 5.5V to 2.4V in 1V/us V_{OUT} = 1.2V Load = 10mA

Figure 9-18. Line Regulation

V_{IN} = 2.4V to 5.5V to 2.4V in 1V/us V_{OUT} = 1.2V Load = 10A

Figure 9-19. Line Regulation

V_{IN} = 5.0V V_{OUT} = 1.2V BOM = 2 × 22uF PFM, No Load

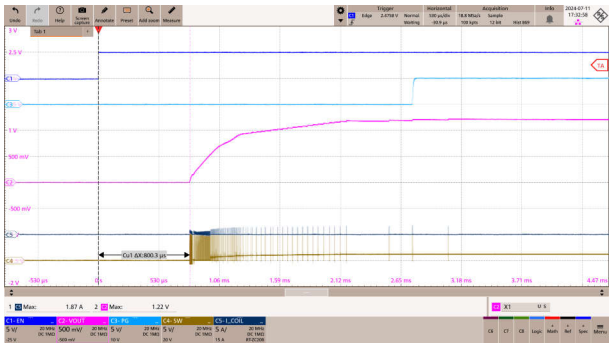
Figure 9-20. PFM Operation

V_{IN}= 5.0V V_{OUT}= 1.2V BOM = 2 × 22uF FPWM, No Load

Figure 9-21. FPWM Operation

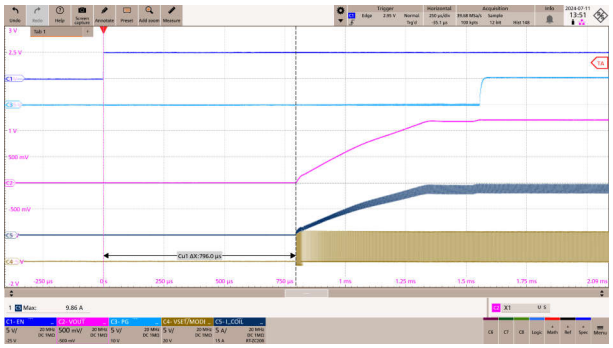
V_{IN} = 5.0V BOM = 2 × 22uF
V_{OUT} = 1.2V FPWM, I_{OUT} = 6A

Figure 9-22. FPWM Operation



TPS6286A06 V_{OUT} = 1.2V No Load

Figure 9-23. Start-up With No Load



TPS6286B10 V_{OUT} = 1.2V Load = 10A

Figure 9-24. Start-up into Full Load

V_{IN} = 5.0V BOM = 2 × 22uF
V_{OUT} = 1.2V I_{OUT} = 10mA to 6A

Figure 9-25. Load Transient - PFM Operation

V_{IN} = 5.0V BOM = 2 × 22uF
V_{OUT} = 1.2V I_{OUT} = 10mA to 6A

Figure 9-26. Load Transient - FPWM Operation

V_{IN} = 5.0V BOM = 2 × 22uF
V_{OUT} = 1.2V I_{OUT} = 3A to 6A

Figure 9-27. Load Transient - FPWM Operation

ADVANCE INFORMATION

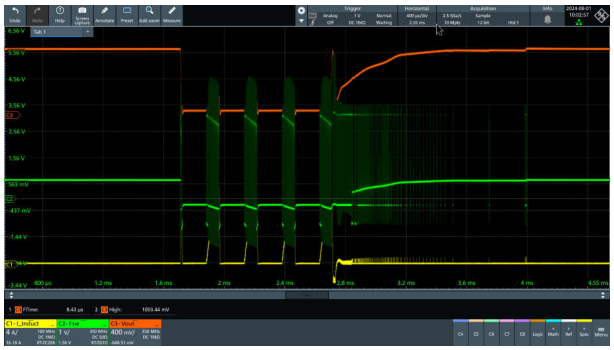


Figure 9-28. HICCUP Short-Circuit Protection

9.3 Power Supply Recommendations

The device is designed to operate from an input voltage supply range from 2.4V to 5.5V. Make sure that the input power supply has a sufficient current rating for the application.

9.4 Layout

9.4.1 Layout Guidelines

A proper layout is critical for the operation of any switched mode power supply, especially at high switching frequencies. The PCB layout of the TPS6286Axx devices requires careful attention to make sure of best performance. A poor layout can lead to issues like bad line and load regulation, instability, increased EMI radiation, and noise sensitivity. Refer to the *Five Steps to a Great PCB Layout for a Step-Down Converter* analog design journal for a detailed discussion of general best practices. The following are specific recommendations for the TPS6286Axx and TPS6286Bxx:

- Place the input capacitor or capacitors as close as possible to the VIN and GND pins of the device. This placement is the most critical component placement. Route the input capacitor or capacitors directly to the VIN and GND pins, avoiding vias.
- Place the output inductor close to the SW pins. Minimize the copper area at the switch node.
- Place the output capacitor or capacitors ground close to the GND pin and route directly, avoiding vias. Minimize the length of the connection from the inductor to the output capacitor. Connect the VOS pin directly to the output capacitor.
- Connect sensitive traces, such as the connections to the VOS, FB, SCL, SDA, and VSEL pins, with short traces and route away from any noise source, such as the SW pin.
- Make the connections from the input voltage of the system and the connection to the load as wide as possible to minimize voltage drops.
- Have a solid ground plane between GND and the input and output capacitor ground connections.
- Connect the sensitive signal ground connections for the feedback voltage divider to a separate signal ground trace.

9.4.2 Layout Example

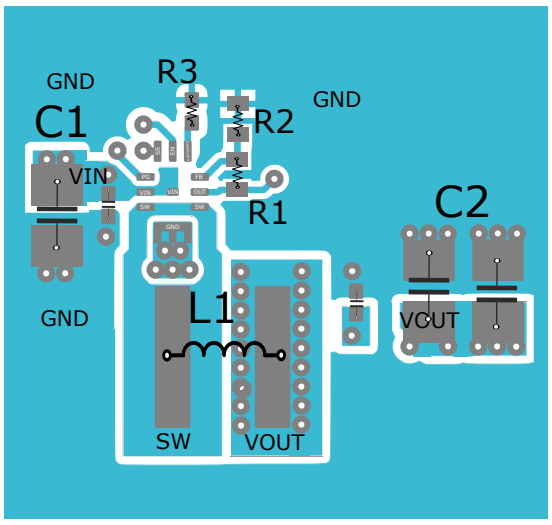


Figure 9-29. Layout Example TPS6286A06

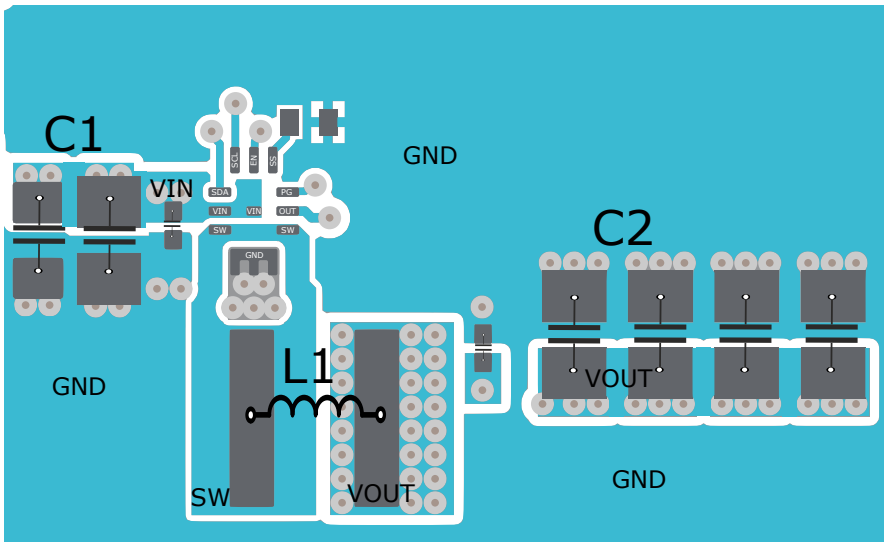


Figure 9-30. Layout Example TPS6286B10

9.4.2.1 Thermal Considerations

After the layout recommendations for component placement and routing have been followed, the PCB design must focus on thermal performance. Thermal design is important and must be considered to remove the heat generated in the device during operation. The device junction temperature must stay below the maximum rated temperature of 125°C for correct operation.

Use wide traces and planes, especially to the GND, VIN, and VOUT pins, and use vias to internal planes to improve the power dissipation capability of the design. If the application allows, use airflow in the system to further improve cooling.

The *Thermal Information* table provides the thermal parameters of the device and the package based on the JEDEC standard 51-7. See the *Semiconductor and IC Package Thermal Metrics* application note for a detailed explanation of each parameter. In addition to the JEDEC standard, the thermal information table also contains the thermal parameters of the EVM. The EVM better reflects a real-world PCB design with thicker traces connecting to the device.

ADVANCE INFORMATION

10 Device and Documentation Support

10.1 Device Support

10.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

10.1.2 Development Support

10.1.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the TPS6286A10, TPS6286A08 and TPS6286A06 devices with the WEBENCH® Power Designer.

Click here to create a custom design using the TPS6286B10 and TPS6286A08 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

10.2 Documentation Support

10.2.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Thermal Characteristics of Linear and Logic Packages Using JEDEC PCB Designs* application note
- Texas Instruments, *Five Steps to a Great PCB Layout for a Step-Down Converter* analog design journal

10.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

10.5 Trademarks

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WEBENCH® is a registered trademark of Texas Instruments.
All trademarks are the property of their respective owners.

10.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.7 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

11 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

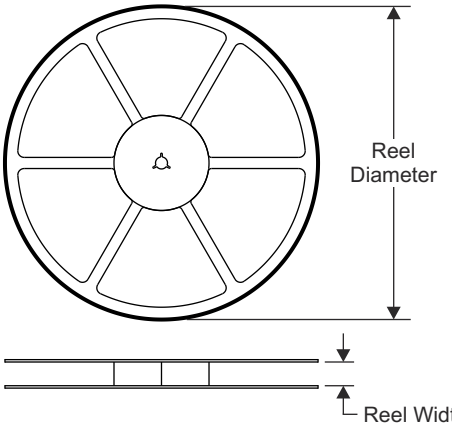
DATE	REVISION	NOTES
September 2024	*	Initial Release

12 Mechanical, Packaging, and Orderable Information

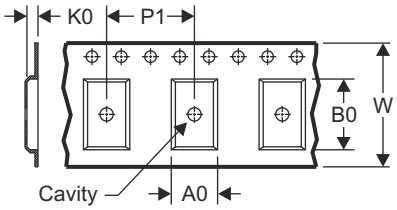
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

12.1 Tape and Reel Information

REEL DIMENSIONS

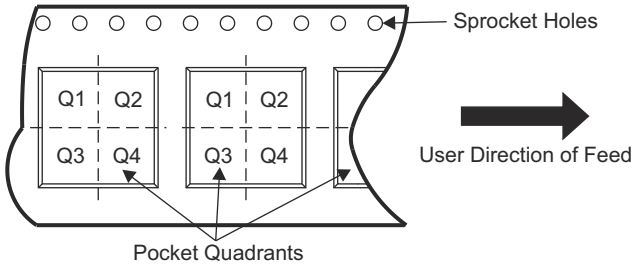


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

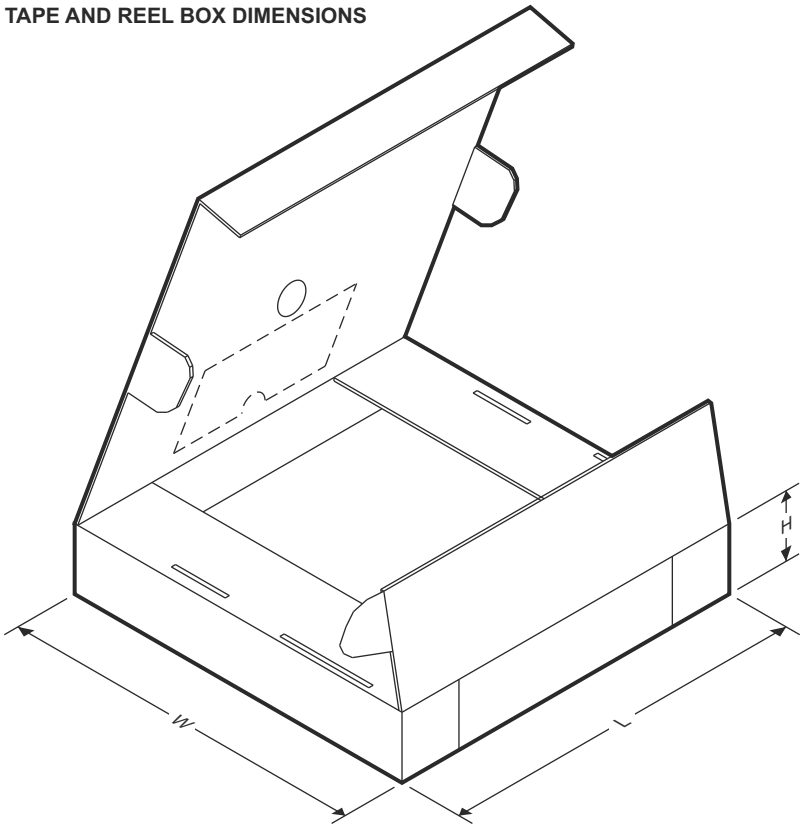


Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS6286A06VBMR	VQFN-HR	VBM	13	3000	180	8.4	2.25	3.25	1.05	4.0	8	Q1
TPS6286B10VBMR	VQFN-HR	VBM	13	3000	180	8.4	2.25	3.25	1.05	4.0	8	Q1

ADVANCE INFORMATION

ADVANCE INFORMATION

TAPE AND REEL BOX DIMENSIONS



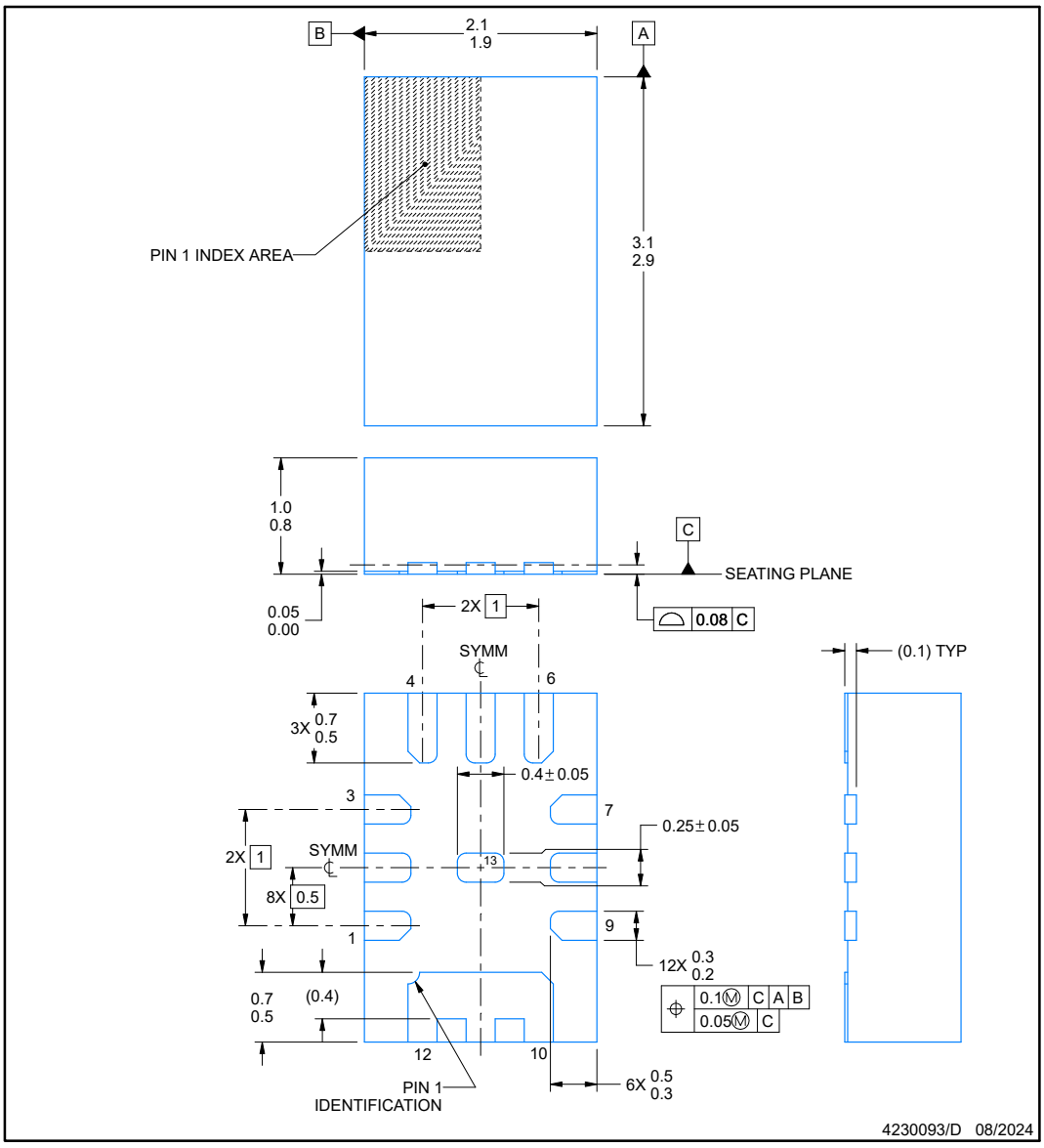
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS6286A06VBMR	VQFN-HR	VBM	13	3000	210	185	35
TPS6286B10VBMR	VQFN-HR	VBM	13	3000	210	185	35

PACKAGE OUTLINE

VBM0013A

VQFN-HR - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

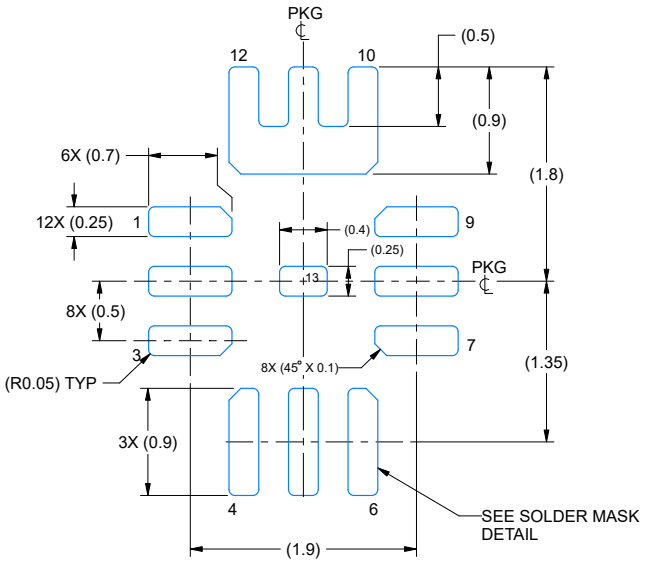
ADVANCE INFORMATION

EXAMPLE BOARD LAYOUT

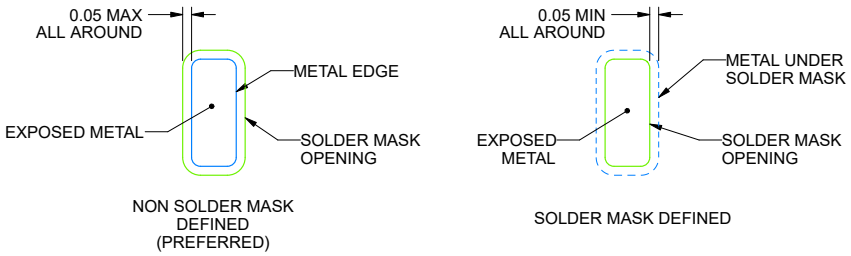
VBM0013A

VQFN-HR - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



SOLDER MASK DETAILS

4230093/D 08/2024

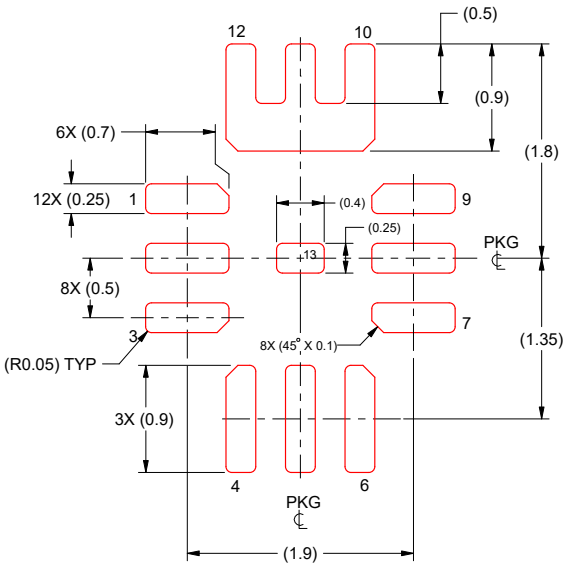
NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

VBM0013A — **VQFN-HR - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.1 MM THICK STENCIL
SCALE: 20X

4230093/D 08/2024

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
XPS6286A06VBMR	ACTIVE	VQFN-HR	VBM	13	3000	TBD	Call TI	Call TI	-40 to 125		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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