

PRECISION MICROPOWER SHUNT VOLTAGE REFERENCE

Check for Samples: [LM4040-EP](#)

FEATURES

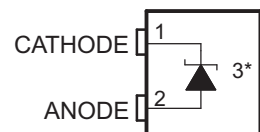
- Fixed Output Voltage of 2.5 V
- Tight Output Tolerances and Low Temperature Coefficient
 - Max 0.65%, 100 ppm/°C
- Low Output Noise: 35 μV_{RMS} Typ
- Wide Operating Current Range: 45 μA Typ to 15 mA
- Stable With All Capacitive Loads; No Output Capacitor Required

APPLICATIONS

- Data-Acquisition Systems
- Power Supplies and Power-Supply Monitors
- Instrumentation and Test Equipment
- Process Controls
- Precision Audio
- Automotive Electronics
- Energy Management
- Battery-Powered Equipment

SUPPORTS DEFENSE, AEROSPACE, AND MEDICAL APPLICATIONS

- Controlled Baseline
- One Assembly/Test Site
- One Fabrication Site
- Available in Military (–55°C/125°C) Temperature Range⁽¹⁾
- Extended Product Life Cycle
- Extended Product-Change Notification
- Product Traceability

DBZ (SOT-23) PACKAGE
(TOP VIEW)


* Pin 3 is attached to substrate and must be connected to ANODE or left open.

(1) Custom temperature ranges available

DESCRIPTION/ORDERING INFORMATION

The LM4040 series of shunt voltage references are versatile, easy-to-use references that cater to a vast array of applications. The 2-pin fixed-output device requires no external capacitors for operation and is stable with all capacitive loads. Additionally, the reference offers low dynamic impedance, low noise, and low temperature coefficient to ensure a stable output voltage over a wide range of operating currents and temperatures. The LM4040 uses fuse and Zener-zap reverse breakdown voltage trim during wafer sort to offer an output voltage tolerance of 0.65%.

Packaged in a space-saving SOT-23-3 package and requiring a minimum current of 45 μA (typ), the LM4040 also is ideal for portable applications. The LM4040C25 is characterized for operation over an ambient temperature range of –55°C to 125°C.

ORDERING INFORMATION⁽¹⁾

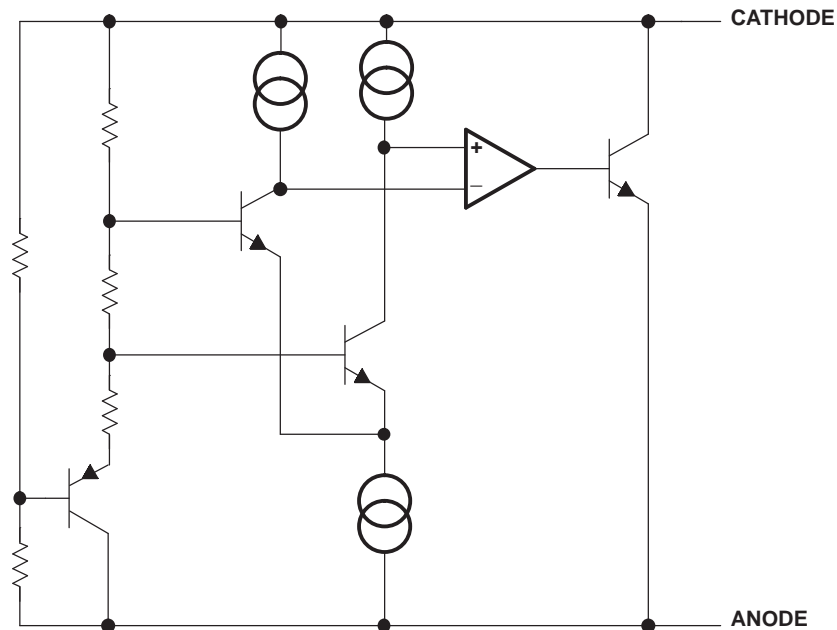
T _A	DEVICE GRADE	V _{KA}	PACKAGE		ORDERABLE PART NUMBER	TOP-SIDE MARKING ⁽²⁾
–55°C to 125°C	0.65% initial accuracy and 100 ppm/°C temperature coefficient	2.5 V	SOT-23-3 (DBZ)	Reel of 250	LM4040C25MDBZTEP	SAGU

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
- (2) The actual top-side marking has one additional character that designates the wafer fab/assembly site.



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FUNCTIONAL BLOCK DIAGRAM

Absolute Maximum Ratings⁽¹⁾

over free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
I_Z	Continuous cathode current	-10	25	mA
T_J	Operating virtual junction temperature		150	°C
T_{stg}	Storage temperature range	-65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

THERMAL INFORMATION

THERMAL METRIC ⁽¹⁾		LM4040	UNITS
		DBZ	
		3 PINS	
θ_{JA}	Junction-to-ambient thermal resistance ⁽²⁾	320.8	°C/W
θ_{JC}	Junction-to-case thermal resistance	98.2	
θ_{JB}	Junction-to-board thermal resistance ⁽³⁾	53.3	
ψ_{JT}	Junction-to-top characterization parameter ⁽⁴⁾	3.3	
ψ_{JB}	Junction-to-board characterization parameter ⁽⁵⁾	51.8	

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(4) The junction-to-top characterization parameter, ψ_{JT} , estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
(5) The junction-to-board characterization parameter, ψ_{JB} , estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).

Recommended Operating Conditions

		MIN	MAX	UNIT
I_Z	Cathode current	See ⁽¹⁾	15	mA
T_A	Free-air temperature	-55	125	°C

(1) See parametric tables

Electrical Characteristics

at extended temperature range, full-range $T_A = -55^\circ\text{C}$ to 125°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
V_Z	Reverse breakdown voltage	$I_Z = 100\ \mu\text{A}$	25°C	2.5		V
ΔV_Z	Reverse breakdown voltage tolerance	$I_Z = 100\ \mu\text{A}$	25°C	-16	16	mV
			Full range	-42	42	
$I_{Z,\text{min}}$	Minimum cathode current		25°C	45	75	μA
			Full range		82	
α_{VZ}	Average temperature coefficient of reverse breakdown voltage	$I_Z = 10\ \text{mA}$	25°C	± 20		ppm/°C
			25°C	± 15		
			Full range		± 100	
			25°C	± 15		
$\frac{\Delta V_Z}{\Delta I_Z}$	Reverse breakdown voltage change with cathode current change	$I_{Z,\text{min}} < I_Z < 1\ \text{mA}$	25°C	0.3	0.8	mV
			Full range		1.1	
		$1\ \text{mA} < I_Z < 15\ \text{mA}$	25°C	2.5	6	
			Full range		9	
Z_Z	Reverse dynamic impedance	$I_Z = 1\ \text{mA}$, $f = 120\ \text{Hz}$, $I_{AC} = 0.1 I_Z$	25°C	0.3		Ω
e_N	Wideband noise	$I_Z = 100\ \mu\text{A}$, $10\ \text{Hz} \leq f \leq 10\ \text{kHz}$	25°C	35		μV_{RMS}
	Long-term stability of reverse breakdown voltage	$t = 1000\ \text{h}$, $T_A = 25^\circ\text{C} \pm 0.1^\circ\text{C}$, $I_Z = 100\ \mu\text{A}$		120		ppm
V_{HYS}	Thermal hysteresis ⁽¹⁾	$\Delta T_A = -55^\circ\text{C}$ to 125°C		0.08		%

(1) Thermal hysteresis is defined as $V_{Z,25^\circ\text{C}}$ (after cycling to -55°C) – $V_{Z,25^\circ\text{C}}$ (after cycling to 125°C).

TYPICAL CHARACTERISTICS

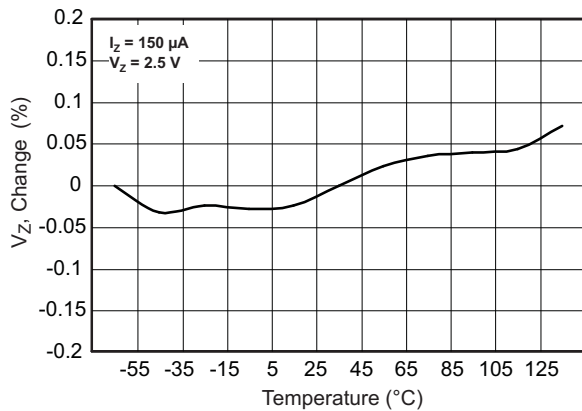


Figure 1. Change in V_Z vs Change in Temperature

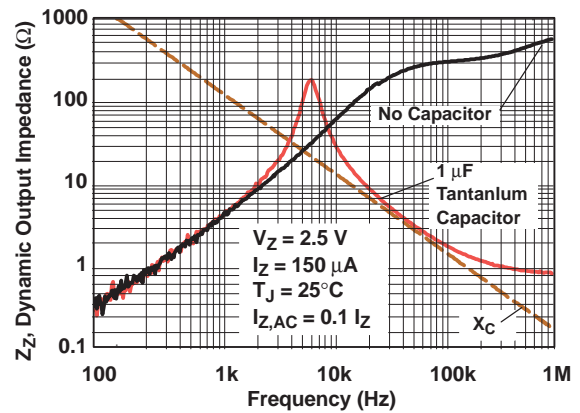


Figure 2. Output Impedance vs Frequency

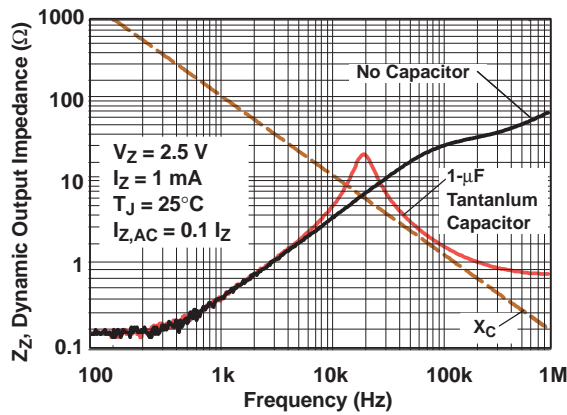


Figure 3. Output Impedance vs Frequency

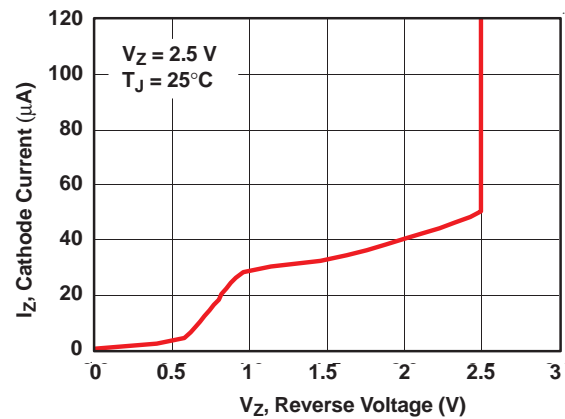


Figure 4. Cathode Current vs Reverse Voltage

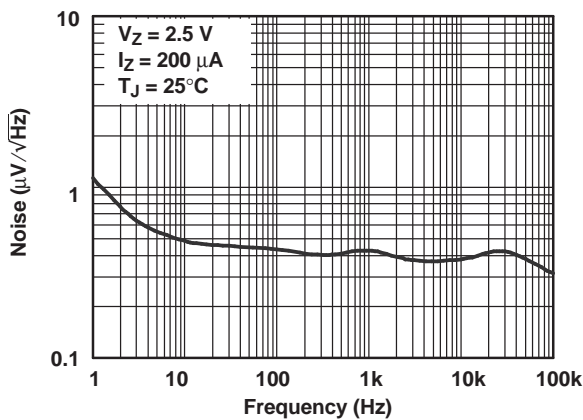


Figure 5. Noise Voltage vs Frequency

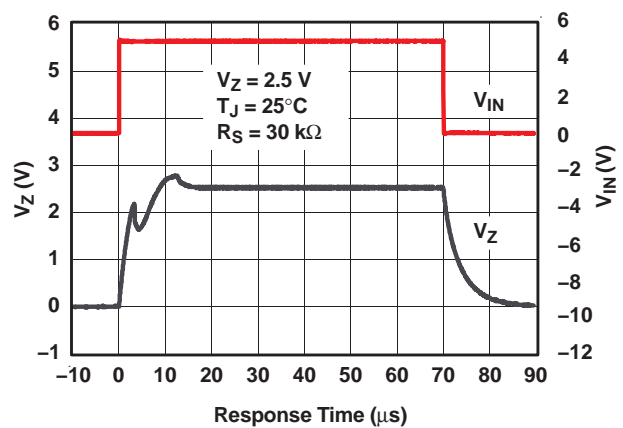


Figure 6. Start-Up Characteristics

APPLICATION INFORMATION

Start-Up Characteristics

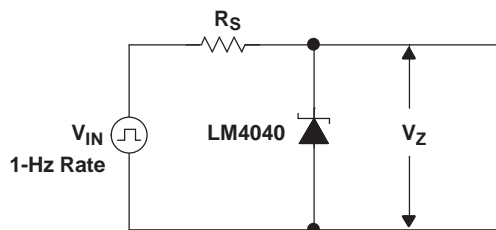


Figure 7. Test Circuit

Output Capacitor

The LM4040 does not require an output capacitor across cathode and anode for stability. However, if an output bypass capacitor is desired, the LM4040 is designed to be stable with all capacitive loads.

SOT-23 Connections

There is a parasitic Schottky diode connected between pins 2 and 3 of the SOT-23 packaged device. Thus, pin 3 of the SOT-23 package must be left floating or connected to pin 2.

Cathode and Load Currents

In a typical shunt-regulator configuration (see [Figure 8](#)), an external resistor, R_S , is connected between the supply and the cathode of the LM4040. R_S must be set properly, as it sets the total current available to supply the load (I_L) and bias the LM4040 (I_Z). In all cases, I_Z must stay within a specified range for proper operation of the reference. Taking into consideration one extreme in the variation of the load and supply voltage (maximum I_L and minimum V_S), R_S must be small enough to supply the minimum I_Z required for operation of the regulator, as given by data-sheet parameters. At the other extreme, maximum V_S and minimum I_L , R_S must be large enough to limit I_Z to less than its maximum-rated value of 15 mA.

R_S is calculated according to [Equation 1](#):

$$R_S = \frac{(V_S - V_Z)}{(I_L + I_Z)} \quad (1)$$

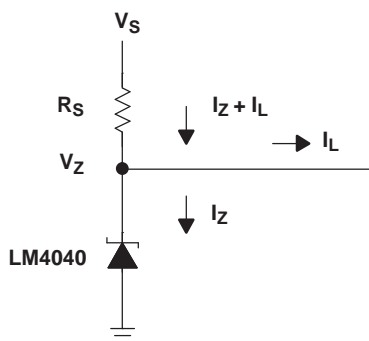


Figure 8. Shunt Regulator

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM4040C25MDBZTEP	ACTIVE	SOT-23	DBZ	3	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	SAGU	Samples
V62/11615-01XE	ACTIVE	SOT-23	DBZ	3	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	SAGU	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM4040C25MDBZTEP	SOT-23	DBZ	3	250	179.0	8.4	3.15	2.95	1.22	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM4040C25MDBZTEP	SOT-23	DBZ	3	250	200.0	183.0	25.0

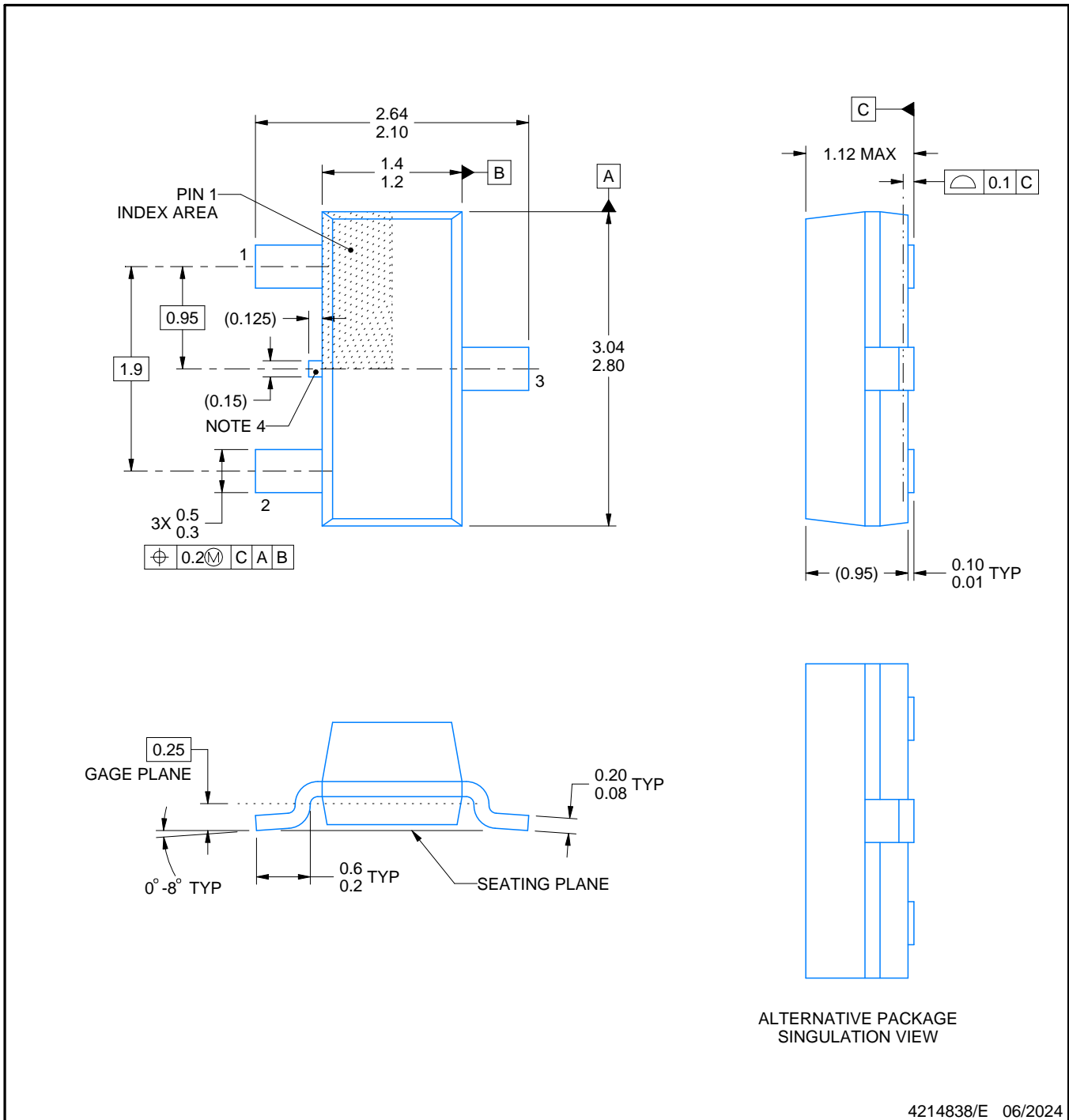
DBZ0003A



PACKAGE OUTLINE

SOT-23 - 1.12 mm max height

SMALL OUTLINE TRANSISTOR



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NOTES:

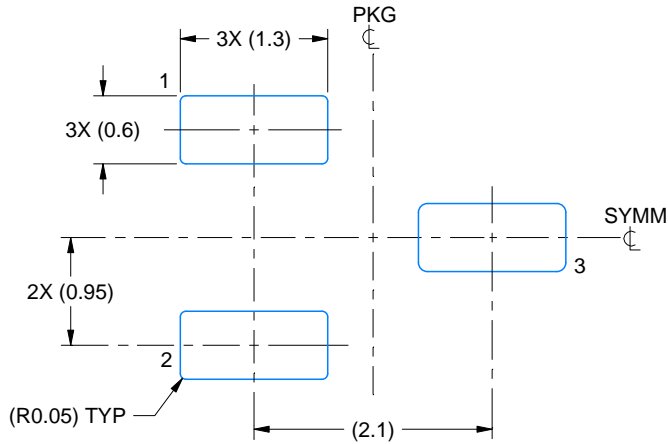
- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- Reference JEDEC registration TO-236, except minimum foot length.
- Support pin may differ or may not be present.
- Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side

EXAMPLE BOARD LAYOUT

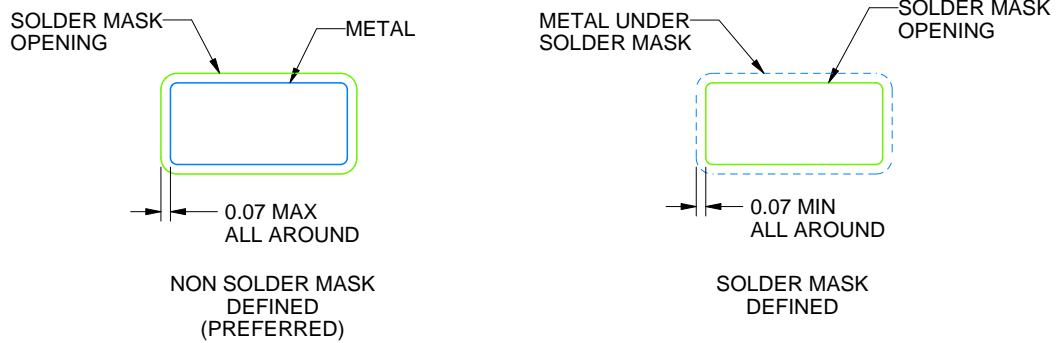
DBZ0003A

SOT-23 - 1.12 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
SCALE:15X



SOLDER MASK DETAILS

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NOTES: (continued)

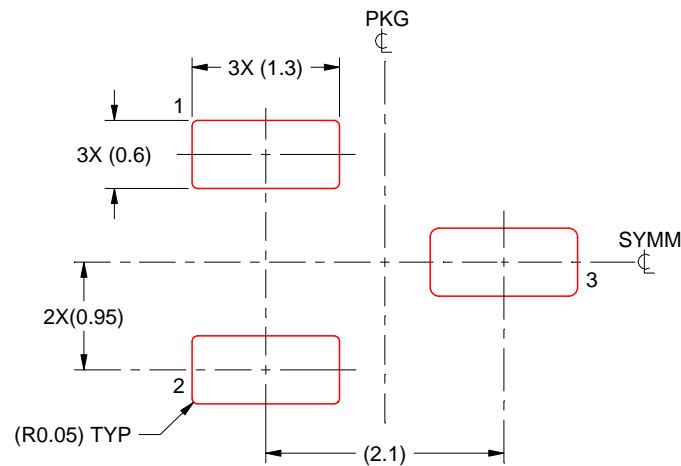
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBZ0003A

SOT-23 - 1.12 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:15X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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